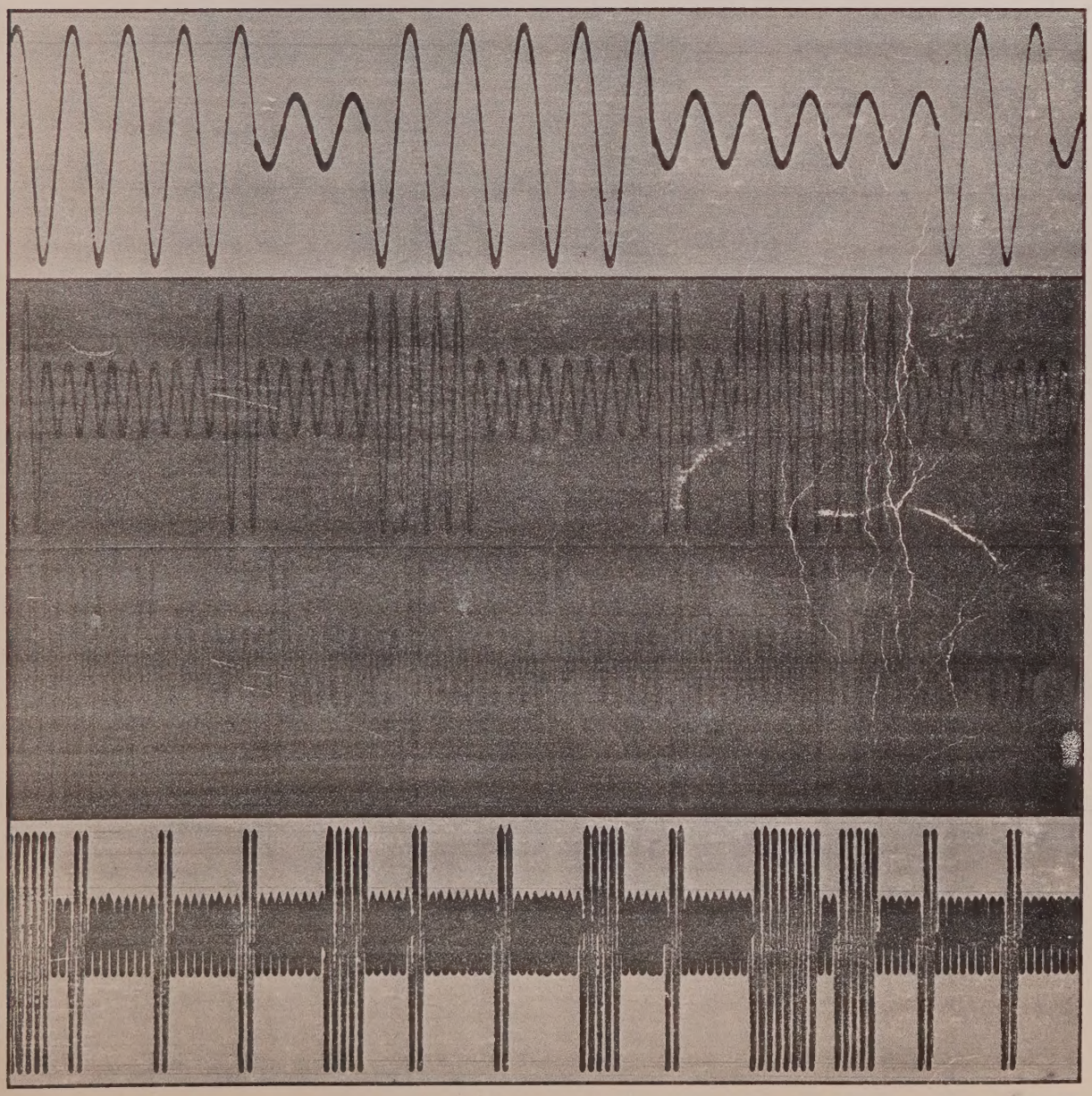
TIMING/SYSTEMS

INSTRUCTION MANUAL

ID No. CH 1276.8
Users Manual
- RETURN TO -
INSTRUMENT CONTROL
SYLVANIA, SES -- West

SD 8120-232
Time Code Generator



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ID No. C/N 17768
Record Manual
- RETURN TO -
INSTRUMENT CONTROL
SYLVANIA SCS -- West

MODEL 8120- 232

TIME CODE GENERATOR

S/N
7-3-970
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ADDENDUM

MODEL 8120
(for Model 8120-232)

This Model 8120 serial number 110 has been factory modified to include the capabilities provided by options:

C13 IRIG C code (100 Hz) in place of IRIG B.

E13 Three digits of switch selectable Days/ID number. Generate/Read.

L17 AC/DC Power Supply.

For Option C13 refer to paragraph 1.6 page 1-6, paragraph 6.8 page 6-31 and page 6-40.

For Option E13 refer to paragraph 1.5 page 1-4, paragraph 6.2 page 6-7 and page 6-40.

For Option L17 refer to paragraph 1.5 page 1-5, paragraph 6.1 page 6-2 and page 6-40.

Additionally the Model 8120-232 has been factory modified to provide remote control of the HOLD and GENerate functions. To accomplish this, the mode switch has had an additional deck and an additional position added.

To connect the remote control, connect the two contacts of a single pole/double throw switch to pins 40 and 42 on J6. The "arm" of the switch should connect to signal ground, pin 48 or 49 on J6.

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The remote control switch will select either HOLD or GENerate when the front panel mode switch is in the REMote position. The time RESET/PRESET switch will not operate when in remote mode.

TABLE OF CONTENTS

			Page
CHAPTER 1	GENERAL DESCRIPTION		
	1.1	Basic Functions	1-1
	1.2	Standard Features	1-1
	1.3	Applications	1-1
	1.4	Specifications	1-2
	1.5	Standard Options	1-4
	1.6	Standard Code Options	1-5
CHAPTER 2	INSTALLATION		
	2.1	Initial Inspection	2-1
	2.2	Storage and Reshipment	2-1
	2.3	Power and Cooling Requirements	2-2
	2.4	Initial Adjustment	2-2
	2.5	Installation	2-3
CHAPTER 3	OPERATION		
	3.1	Operation	3-1
	3.2	Mode Selection	3-1
	3.2.1	Main Power	3-1
	3.2.2	Stop	3-1
	3.2.3	Hold	3-1
	3.2.4	Generate	3-2
	3.3	Preset-Reset Switches	3-2
	3.4	Front Panel Controls and Indicators	3-3
	3.5	Rear Panel Controls and Indicators	3-4
CHAPTER 4	MAINTENANCE AND CALIBRATION		
	4.1	Factory Service	4-1
	4.2	Routine Maintenance	4-1
	4.3	Printed-Circuit Board Repair	4-2
	4.4	Logic Functions	4-3

CHAPTER 4 MAINTENANCE AND CALIBRATION (cont)

4.5	Operational Test and Calibration Procedure	4-7
4.5.1	Recommended Test Equipment	4-7
4.5.2	Power Supply	4-8
4.5.3	Power Supply Regulator	4-8
4.5.4	Oscillator Adjustment	4-8
4.5.5	Generate Function	4-10
4.5.6	Shaper and Modulator	4-10

CHAPTER 5 FUNCTIONAL DESCRIPTION

5.1	General	5-1
5.2	Functional	5-1

CHAPTER 6 CIRCUIT DESCRIPTION

6.1	AC/DC Power Supply	6-2
6.2	3 Digit Accumulator W/Buffers	6-7
6.3	Single Digit Readout	6-11
6.4	Time Base Preset/Reset Control	6-12
6.5	3 Digit Buffered Accumulator/Minor Counter	6-17
6.6	Time-of-Day Accumulator	6-21
6.7	Shaper and Modulator	6-25
6.8	Switchable IRIG DC Code Generator	6-31
6.9	20 Bit Buffer	6-37

LIST OF ILLUSTRATIONS

Assembly and Schematic No.	Description	Page
31319-4-1	Switching Regulator	6-5
31320-4-1	Switching Regulator	6-5
31357-7-1	AC/DC Power Supply	6-6
21547-4-8	.3 Digit Accumulator W/Buffers	6-9
21547-7-8	3 Digit Accumulator W/Buffers	6-10
21211-7-1	Single Digit Readout	6-11
21555-4	Time Base Preset/Reset Control	6-15
21555-7-6	Time Base Preset/Reset Control	6-16
21547-4-7	3 Digit Buffered Accumulator/ Minor Counter	6-19
21547-7-7	3 Digit Buffered Accumulator/ Minor Counter	6-20
21543-4-3	Time-of-Day Accumulator	6-23
21543-7-3	Time-of-Day Accumulator	6-24
21556-4-6	Shaper and Modulator	6-29
21556-7-1	Shaper and Modulator	6-30
21554-4-1	Switchable IRIG DC Code Generator	6-35
21554-7-1	Switchable IRIG DC Code Generator	6-36
21535-4-3	20 Bit Buffer Non-Inverting	6-38
21535-7-3	20 Bit Buffer Non-Inverting	6-39
31356-7-1	Wiring Block Diagram	6-40
	Optional Codes and Code Formats	6-41 thru 6-44

CHAPTER 1

GENERAL DESCRIPTION

1.1 BASIC FUNCTIONS

The Model 8120 Time Code Generator is designed to generate an Inter Range Instrumentation Group B, (IRIG B), time-code format in terms of Binary Coded Decimal (BCD) hours, minutes, and seconds.

As a Time Code Generator, the Model 8120 is a precise digital clock, which also generates a serial code for use in recording continous time on magnetic tape or for central timing applications.

1.2 STANDARD FEATURES

The Model 8120 is designed for simple, reliable operation and ease of maintenance. Its circuitry is designed to make full use of integrated circuits whenever possible and is constructed on printed-circuit plug-in modules.

In the Generate Mode, the Model 8120 can be used to provide Real Time or Elapsed Time operation thus providing maximum flexibility in timekeeping and during data recordings.

1.3 APPLICATIONS

In addition to the functions described in Section 1.1, the Model 8120 generates a DC Level Shift signal as well as four precisely controlled pulse rates. Time information is also supplied in the form of 20 parallel BCD lines (32 lines when day option included) for use with a digital recorder or for computer interface applications.

Updated time is displayed on an in-line readout in terms of hours, minutes, and seconds.

1.4 SPECIFICATIONS

TIME BASE

Crystal controlled ocsillator with an aging rate of 1 part in 10^7 per day and an over all stability of 1 part in 10^5 per day from 0° to 60°C. Provisions are included for the use of an external 1 MHz time base.

DISPLAY

Six digit in-line readout to indicate time of day in hours, minutes, and seconds (three additional digits of Day-of-Year Days) Run Number (ID) option is included.

CODE FORMAT

Modified IRIG B format in terms of BCD hours, minutes, and seconds(Day-of-Year or Run Number optional).

OUTPUTS (All outputs are short circuit proof to ground):

Modulated Code

The modulated code is generated on a 1 kHz carrier with an adjustable amplitude from 0 to 10 volts peak-to-peak from a low impedance 15 mA source and an adjustable modulation ratio (Mark-to-Space) from 2:1 to 6:1. Connector is rear panel BNC type.

DC Level Shift Code

The DC Level Shift code is generated with an adjustable amplitude from 0 to 10 Volts into a minimum 600 Ω Load. Connector is rear panel BNC type.

Pulse Rates

Simultaneous rates of 1p/s, 10 p/s, 100 p/s, and 1,000 p/s are provided with leading edge "on time". Levels are 0 to +5 volts (nonimal) from a 6 kΩ source. Connector is rear panel Amphenol 57-40500. The 1pps signal is [illegible]

Parallel BCD Outputs

Updated time is provided as 20 parallel BCD lines representing hours, minutes, and seconds (32 parallel lines if days option is included).

Code: 8-4-2-1

Logic: Binary "1" = 5 (±0.5) volts, 6 kΩ source.
Binary "0" = 0 (±0.5) volts, 15 mA sink.

Connector: Amphenol 57-40500

INPUTS:

External Time Base

Accepts a 1 MHz (nonimal) input at 1 volt peak-to-peak (nonimal) into 1 kΩ, via a rear panel BNC type connector. A rear panel switch selects INTernal or EXTernal time base.

Elapsed Time Command

A +5 V level to count or a ground condition to inhibit time advance.

MANUAL CONTROLS

Mode: Rotary switch to select POWER OFF, STOP, HOLD and GENERATE.

Time Set: Six thumbwheel switches for selecting initial start time in hours, minutes and sceonds (three additional thumbwheels for Day-of-Year or Run Number options).

Preset/Reset: Momentary toggle switch to preset selected time or to reset time to zero. When Day of Year or Run Number option is included, a separate Preset/ Reset switch is provided to allow changing day or run number without interrupting time accumulation.

Time Base: Rear Panel switch to select internal or external time base.

ENVIRONMENT:

0° to 60°C at up to 95% relative humidity.

POWER:
117/230 volts (±10%), 48 to 62 Hz at less than 55 watts. 48 to 440 Hz operation is optional.

PACKAGE:
3 1/2 inches high by 19 inches wide X 17 inches deep (8.9 X 48.3 X 38cm). Removable rack flanges Feet, tilt stand, and trim kit supplied for bench top operation. Chassis is drilled for Chassis Trak CTS-120 series slides. Weight is approximately 23 pounds (6.2 kg.).

1.5 STANDARD OPTIONS:

OPTION A12-A Slow Code A
Provides Type A Slow Code output for grahpic recorders. Nine selectable rates. Hours, minutes, and seconds.

OPTION A12-B Slow Code B:
Provides Type B Slow Code output for graphic recorders. Nine selectalbe rates. Days, hours, minutes, and seconds.

OPTION B13 High Stability Oscillator:
High-stability heated oscillator with stability of 5×10^{9} per day from 0° to 60°C.

OPTION B14 Zero Warm-up Oscillator:
Zero warmup, temperature compensated oscillator with stability of 2×10^{-9} per day at constant temperature and 2×10^{-7} per day from 0° to 60°C.

OPTION D12 Positive BCD Buffers:
Provides (positive true) BCD buffered outputs.

OPTION D13 Negative BCD Buffers:
Provides (negative true) BCD buffered outputs.

OPTION E13 Day-of-Year/Run Number
The Day-of-Year/Run Number Option provides the capability of presetting, displaying, generating, and reading the three digits of the Day-of-Year portion of the code (000-999). A rear panel switch will allow the operator to substitute a three digit Run Number or ID number for the Day-of-Year information via a rear

panel BNC connector.

OPTION E14 Milliseconds:

Adds milliseconds information to BCD.

OPTION L12 400 Hz power:

117/230 volt, 48 to 440 Hz operation.

OPTION L17:

Ac/dc power supply permits operation from 115/230 V ac 60 Hz or 20-50 V dc (24-28 V dc nominal).

OPTION S11 External Synchronization

Provides external time synchronization including precision advance/retard capability.

OPTION S11 A WWV Synchronization

Provides full WWV Synchronization capability including Propagation Delay.

Note: OPTION S11-S11 A Synchronization:

In the Generate Mode, the Model 8120 can be used to provide real time or Elapsed Time operation to provide maximum flexibility in timekeeping and during data recording. External time synchronization capability including precision advance/retard control is also provided. Neon lamps indicate synchronization accuracy to within a few milliseconds of an incoming WWV signal without the use of an external oscilloscope.

1.6 STANDARD CODE OPTIONS

The 8120 can be supplied to read any one of the standard IRIG, NASA or XR3 code formats cited in Table 1-2 in place of IRIG B or in addition to IRIG B.

The 8120 can also be supplied as a universal IRIG code translator to read any of the IRIG codes cited in Table 1-2 and the standard IRIG B code.

TABLE 1-2

STANDARD CODE OPTIONS

Option No.	Description
C11	IRIG A Code (10 kHz) in place of IRIG B
C13	IRIG C Code (100 Hz) in place of IRIG B
C13A	IRIG C Code (1 kHz) in place of IRIG B
C14	IRIG D Code (100 Hz) in place of IRIG B
C15	IRIG E Code (100 Hz) in place of IRIG B
C15A	IRIG E Code (1 kHz) in place of IRIG B
C17	NASA 28 Code (100 Hz) in place of IRIG B
C18	NASA 36 Code (1 kHz) in place of IRIG B
C26	XR3 Code (250 Hz) in place of IRIG B
C26A	XR3 Code (1 kHz) in place of IRIG B
C40	Universal IRIG codes (except IRIG D)

CHAPTER 2
INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect the instrument for any damage and if shipping damage is found, refer to the warranty inside the rear cover of this manual, and to sub-section 2.2 for repacking and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. The test given in the overall maintenance sub-section is recommended for this purpose. Should the instrument fail to meet specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)
Minimum Temperature: -69°F (-55°C).

To protect your instrument during shipment or storage, use the best packing methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packing. Contract packing companies can provide dependable packaging on short notice.

General packaging instructions:

(1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

(2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb./sq. in. bursting strength) or a wooden box to house the instrument.

(3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

(4) Seal the package with strong tape or metal bands. Mark with "Delicate Instrument".

(5) Refer to the warranty inside the rear cover of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by model number and full serial number.

2.3 POWER AND COOLING REQUIREMENTS

The Model 8120 can operate from 115 V or 230 V ± 10%. 48 to 62 Hz. It is normally supplied for 115 volt operation.

To adapt the Model 8120 to 230 volt usage, remove the jumper wire between pins 1 and 2 and also pins 3 and 4 of the main power terminal board (on rear panel). Install a jumper wire between pins 2 and 3 of the main power terminal board.

CAUTION

DISCONNECT ALL POWER FROM THE UNIT BEFORE CHANGING VOLTAGES.

2.4 INITIAL ADJUSTMENT

To apply primary power to the Model 8120, it is only necessary to turn the four position mode switch to PWR OFF, install the power cord (supplied) and turn the switch to GENerate.

The EXT-INT switch on the rear panel must be in INT position to utilize the internal 1 MHz oscillator. If the use of an external 1 MHz source is desired, the switch must be in the EXT position.

Modulated Code Amplitude Adjustment Control on Card A3 (a 100 kΩ potentionmeter) must be adjusted to the input voltage required by the particular tape transport in use (1 volt peak-to-peak is standard). Voltage may be observed at MOD JACK or at the MOD test point on A3.

The Modulation Ratio Control (a 5 kΩ potentionmeter) has been factory adjusted for 3/1 modulation ratio and should not require further adjustment. If adjustment should become necessary, the ratio control on Card A3 may be adjusted as desired.

If the Level Shift output is also to be used, R23 on A3 (marked as DC) may be adjusted for the desired output level. R23 will adjust the Level Shift out from ground to +10 V dc.

2.5 INSTALLATION

The unit is normally supplied for bench top and tilt stand operation. If standard rack mounting is desired the following steps are necessary.

(1) Remove two screws and molding from both sides of the unit.

(2) Remove and retain two side trim panels.

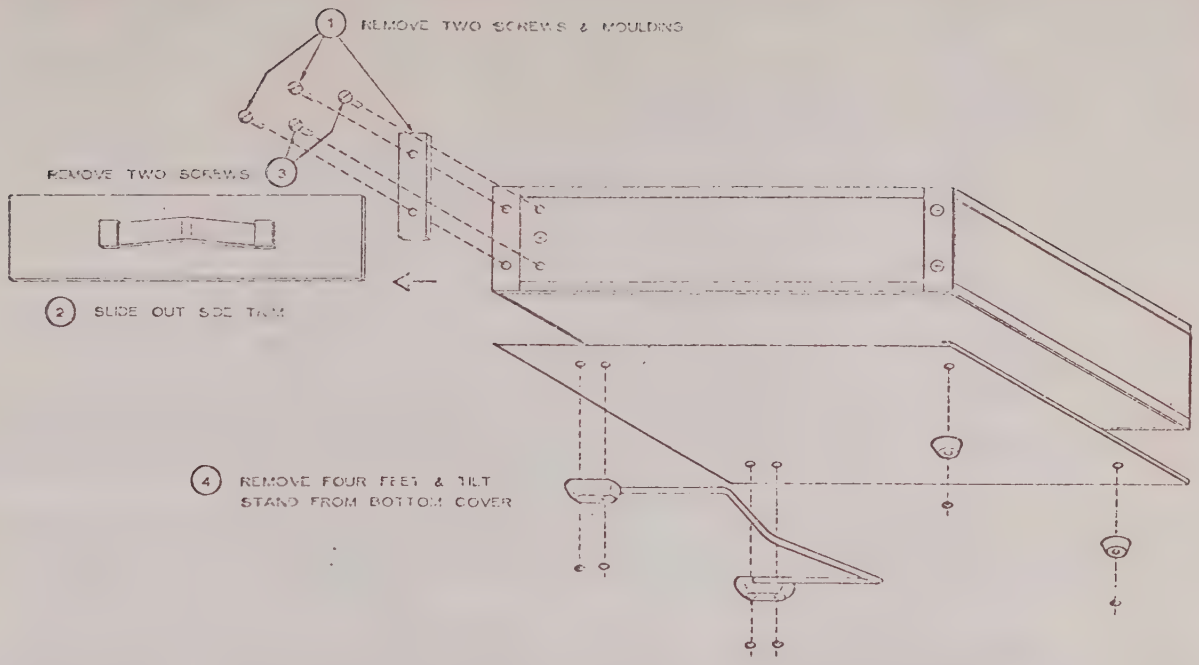
(3) Remove two screws from both side panels.

(4) Remove and retain the feet and tilt stand from bottom cover.

(5) Install mounting ears (supplied) on both side panels as shown.

(6) Install slide assembly and spacers as shown (supplied).

For convenience, the Model 8120 has been drilled for



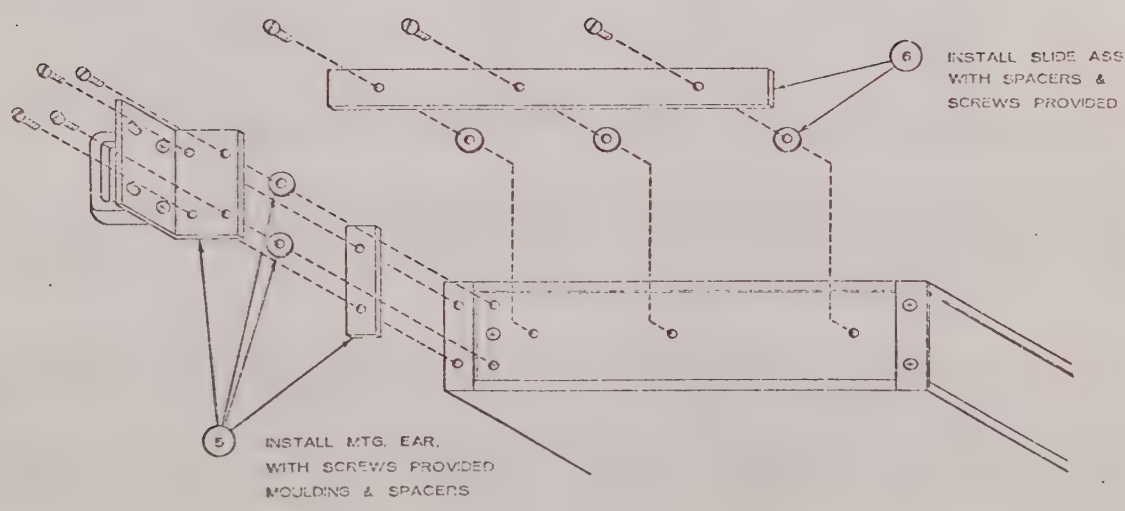


FIGURE 2.2
RACK MOUNTING

Chassis Trak CTS-120 series slides.

If the unit is to be bench mounted, the air intake holes in the bottom of the chassis must not be obstructed. If the unit is to be rack mounted, the air intake holes in the sides of the chassis must not be obstructed.

NOTE

Under no conditions should air outlet hole in the rear of the unit be obstructed.

CHAPTER 3

OPERATION

3.1 GENERAL

The Model 8120 is ready to operate immediately after turning on the power switch. Preliminary adjustments or calibration procedures are not normally required. It is advisable to read the following description, which describes the use of the controls and indicators, before using the unit.

3.2 MODE SELECTION

A four position front panel switch controls the main power and the basic modes of the Model 8120. The modes are stop, preset and GENerate.

3.2.1 Main Power

The PWR OFF position removes all power to the unit except line voltage to the ten position switch and the line fuses.

3.2.2 STOP

The stop position energizes the T.O.Y. (Time-of-year) PRESET-RESET switches. In this position the code generator and minor counters are placed into a "Stop" condition where no outputs are generated.

3.2.3 HOLD

The HOLD position will stop the count in the display register if previously in generate and will allow the latest count to be displayed continuously and the code for this time will be

generated continuously without updating. The PRESET-RESET switches are energized to allow presetting to desired T.O.Y.

3.2.4 GENerate

The GENerate position is used for normal operation. In this position normal updated time is displayed, and the IRIG B code is generated. If the unit has an SII or SIIA Option after a stop condition, either the manual start or auto start momentary switch must be activated.

NOTE

When the mode selection switch is moved from STOP to HOLD, the code generation remains inhibited. When moved from GENerate to HOLD, code generation is normal, except that each frame will contain the same time information, since update does not take place in HOLD.

3.3 PRESET-RESET SWITCHES

When the PRESET-RESET switches are placed in the RESET position the count in the DISPLAY COUNTERS will clear. When the switch is placed in the PRESET position the count in the THUMBWHEEL SWITCHES will automatically be placed in the DISPLAY COUNTERS. The T.O.D. (Time-of-Day) PRESET-RESET switch is armed only when the mode switch is in HOLD or STOP: on units equipped with days the DAYS PRESET-RESET switch is armed at all times.

3.4 FRONT PANEL CONTROLS AND INDICATORS

(1) THUMBWHEEL SWITCHES - The number preselected in the THUMBWHEEL SWITCHES will be preset into the DISPLAY COUNTERS when the PRESET/RESET switch is elevated and the mode selection switch is in the HOLD or STOP position.

(2) DISPLAY COUNTERS - The nine digit DISPLAY COUNTER will continuously display the internally generated time of year.

(3) DAYS PRESET/RESET Switch - This switch will clear, when depressed, the three digit days section of the DISPLAY COUNTER. When elevated it will preset the three digits to the number selected in the THUMBWHEEL SWITCHES (see Section 3.3)

(4) TIME PRESET/RESET Switch - This switch will either clear the six digits of the DISPLAY COUNTER when in reset or it will preset them when elevated (See Section 3.3) if the mode selection switch is in the PRESET or STOP positions.

(5) MODE SELECTION - The four-position mode selection switch controls the main power to the unit as well as the basic modes of operation (See Section 3.2).

(6) TICK LAMP - The TICK LAMP will light once per second whenever a suitable WWV signal is supplied for synchronizationtion purposes.

(7) ON TIME Lamp - The ON TIME lamp will flash whenever the GENerator 1 pps is in exact synchronism with an incoming WWV Tick signal. When AUTO-START mode is used, this indication shows proper starting with the external signal.

(8) AUTO START-MAN START Switch - The three position toggle switch permits either of two starting modes, when mode selection switch is in GENerate, when momentarily depressed, the unit is started manually, the count advancing in the DISPLAY COUNTER one second later. When held in the elevated position, an incoming WWV signal as indicated on a flashing TICK lamp will start the unit and synchronism with WWV will be indicated by the simultaneous flashing of the ON Time Lamp.

3-5 REAR PANEL CONTROL AND INDICATORS

(1) AUXILIARY POWER JACK - Provides auxiliary 115 V ac power for a companion Model 8140 Tape Search Unit.

(2) POWER CORD RECEPTACLE - For use with the AC power cord (supplied).

(3) MILLISECONDS - Provides parallel BCD milliseconds information when Option 14 is installed.

(4) REMOTE CONTROL - Not used.

(5) INTERCONNECT 1 - Provides BCD Time-of-Day and Control signals to Model 8140 Tape Search Unit, and may be used for remote display.

(6) EXT/INT 1 MHz REF. SWITCH - When in the INTernal position, the unit utilized the internal 1 MHz oscillator. In the EXTernal position the internal reference is disabled and an external standard may be used.

(7) 1 MHz REFERENCE - For use with Item 6.

(8) CODE IN - Input jack for the code from the tape unit.

(9) DC CODE - Output jack for the internally generated DC Level Shift code.

(10) SLOW CODE - Output jack for the slow code (Option A12 or A12B).

(11) CODE OUT - Output jack for the internally generated code in the GENerate mode.

(12) PARALLEL OUT and PULSE RATES - This connector supplies Time-of-Day information, in BCD form, and four pulse rates: 1 p/s, 10 p/s, 100 p/s, and 1 k p/s, as well as other signals and voltages. It may be used for remote display and other applications.

CHAPTER 4

MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

Whenever the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns when necessary. Address all inquiries on operation or applications to your nearest sales representative, or to:

Sales Manager
Data Products Division
Systron-Donner Corporation
888 Galindo Street
Concord, California 94520

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for routine maintenance and inspection every five to six months is recommended for this unit (the oscillator may require calibration at more frequent intervals). As part of these regular procedures, the instrument should be checked in the following manner:

(1) Disconnect ac power and remove the top and bottom covers.

(2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

(3) Check for physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage.

When a printed circuit board contains integrated circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

(4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

(5) If the internal panel surfaces and companents have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove the foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

(6) Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints, and other foreign material.

(7) Replace the top and bottom covers and recommect ac power. Perform the Operational Test and Calibration Procedure (Paragraph 4.5). If performance does not match or exceed the specifications listed in Chapter I of this manual, corrective maintenance is in order.

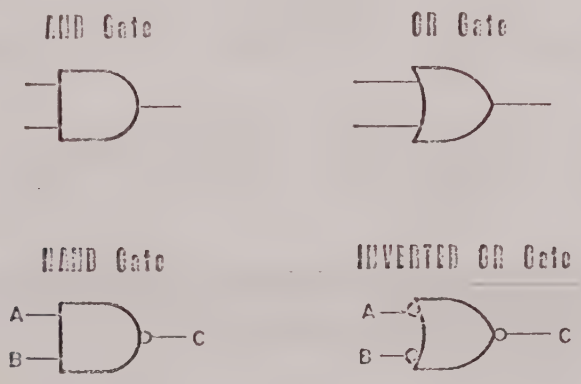
4.3 PRINTED-CIRCUIT BOARD REPAIR

To remove a part on a printed circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts or less) soldering iron, apply heat sparingly to each cut lead.

A soon as the solder melts, slip the lead from the hole and clean the hole with a toothpick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16 inch beyond the back surface of the board. Only 63/37 solder with a maximum diameter of 1/16 inch should be used. Solder the leads to the board and use a hemostat, long-nose pliers, or other heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

4.4 LOGIC FUNCTIONS

The logic symbols and functions, as used in the Model 8120, are described in the following paragraph. Truth tables and detailed explanations are given where necessary in order to assist qualified maintenance personnel in the repair and upkeep of the instrument.



The NAND Gate and the INVERTED OR Gate have the same truth tables.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

INVERTED AND Gate

The NOR Gate and the INVERTED AND Gate have the same truth tables.

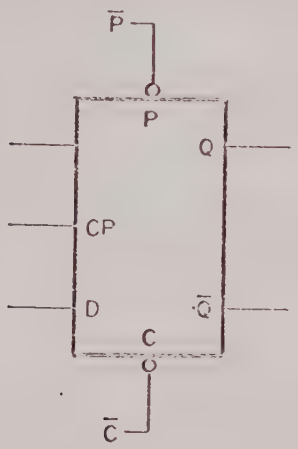
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

DOT AND

DOT OR

In some configurations it is possible to perform the AND and OR function simply by tying the outputs of certain gates together. These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line, the AND or OR symbol is used only once.

D-TYPE Flip-Flop



(1) Q assumes the state of the D input on the positive transition of the clock (CP) input.

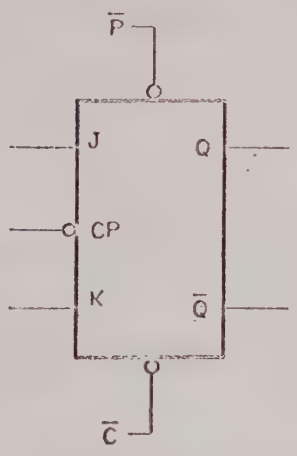
(2) The D input is locked out when the clock input is positive.

(3) P and C override all other inputs.

(4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.

(5) At a preset condition, Q is a Logic 1. At a clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



$J = J1 \cdot J2 \cdot J3$

$K = K1 \cdot K2 \cdot K3$

(1) If J and K are both at Logic 0 when the clock input ($\overline{CP}$) assumes a Logic 0 state there is no change in the output.

(2) If K is a Logic 1, Q will assume a Logic 0 when $\overline{CP}$ goes to Logic 0.

(3) If J is a Logic 1, Q will assume a Logic 1 when $\overline{CP}$ goes to Logic 0.

(4) If J and K are both at Logic 1 the flip-flop will change state when $\overline{CP}$ goes to Logic 0.

(5) The J and K inputs are locked out when the clock input is Logic 0.

(6) $\overline{P}$ and $\overline{C}$ override all other inputs.

(7) If $\overline{P}$ and $\overline{C}$ are both at Logic 0 the Q and $\overline{Q}$ outputs are both at Logic 1.

(8) At a preset condition, Q is a Logic 1. At a clear condition, Q is a Logic 0.

4.5 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the technician to isolate the trouble to a particular circuit card.

When the trouble is isolated to a card, the card description in Chapter 6 will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply and display circuits of this equipment. Use caution at all times when the protective covers are removed.

4.5.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8120.

Model	Manufacturer	Description
531A	TEKTRONIX, INC.	Oscilloscope 15 MHz B Bandwidth triggered sweeps from 0.1 micro-seconds/cm to 5 sec/cm.
CA	TEKTRONIX, INC.	Dual-Trace Calibrated preamp for 531A scope, .05 volts/cm to 20 volts/cm.
P6000	TEKTRONIX, INC.	Probe, 10:1 Attenuation Ratio, 12 pf capacitance.
9000	SYSTRON-DONNER CORP.	VOM, 10 MΩ input impedance, ±0.1% accuracy.
1037	SYSTRON-DONNER CORP.	Frequency Counter, 0 Hz to 50 MHz, 5 parts/10 per week.

4.5.2 Power Supply Dwg. #21445-7

The voltage checks listed below will insure the correct operation of the power supply assuming a normal line voltage of 117 V ac. The voltages listed are not adjustable. The test points are available on the unit chassis.

(1) Insure the presence of +210 V dc at fuse F3.

(2) Insure the presence of +21 V dc at the collector of Q1.

(3) Insure the presence of -21 V dc at the collector of Q2.

(4) Insure the presence of +9 V dc at the collector of Q3.

4.5.3 Power Supply Regulator Dwg. #21409-7

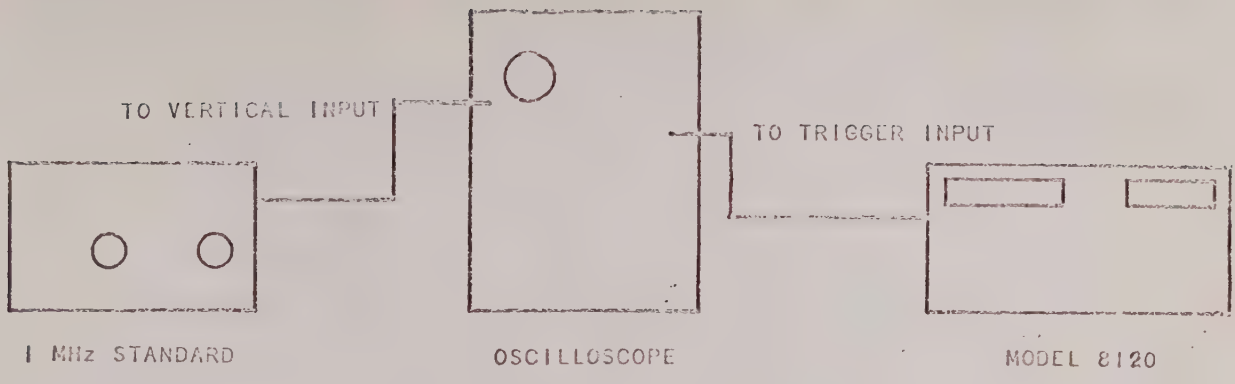
Adjust the following voltages on the regular board:

Voltage	Adjust	Test Point
+15 V ± 0.5 V	R21	Fuse F6
-15 V dc ± 0.5 V	R16	Fuse F5
= 5 V dc ± 0.5 V	R4	Fuse F4

If the Power Supply Regulator card is operating normally and the Power Supply voltages are correct, the above voltages may be obtained with very little difficulty. If the voltages will not adjust properly or fail to maintain their regulation, corrective maintenance is in order.

4.5.4 Oscillator Adjustment

The accuracy of the oscillator may be determined, relative to a frequency standard, by observing the rate of drift of an oscilloscope pattern as shown in Figure 4.1, the oscillator accuracy test diagram.



OSCILLATOR ACCURACY TEST

FIGURE 4-1

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the patern moves to the left, the frequency under test is too high.

To check oscillator frequency (not stability):

(1) Trigger the oscilloscope externally with the 1 MHz internal oscillator of the 8120.

(2) Connect a 1 MHz frequency from an external standard to the vertical input of the oscilloscope.

(3) Set the oscilloscope sweep time to 0.1 μsec/cm and adjust the controls to obtain a presentation of a 5 V peak-to-peak waveform.

(4) Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10^7. If necessary adjust the oscillator (C3, Time Base Preset/Reset card) until drift is negligible.

TABLE 4.2

Oscillator Accuracy

Drift	Accuracy
1 cm/0.1 sec	1 part in 10^6 (10 Hz)
1 cm/sec	1 part in 10^7 (1.0 Hz)
1 cm/10 sec	1 part in 10^8 (0.1 Hz)

4.5.5 Generate Function

(1) Place the mode selection switch in GENerate position and insure that the DISPLAY COUNTER indexes in a normal sequence.

(2) Preset 23 hours 59 minutes 59 seconds into the DISPLAY COUNTER and note that on the next count the display will become all 0's (and, if the instrument displays days, that the days register advances to 001).

(3) Repeat Step #2 and preset 009 in the Days Register and observe that on the next count the days register will advance to 010.

(4) Repeat Step #3 to insure the correct operation of the remaining digit of the days register.

4.5.6 Shaper & Modulator Dwg #21556-7-3 or -4

(1) Adjust the TUNE (R33) control for maximum ac signal at the MOD test point.

(2) Adjust the MOD (R20) control for a nominal 3 V peak-to-peak output of the Large Cycle signal.

(3) Adjust the RATIO (R16) control for a 3/1 modulation ratio.

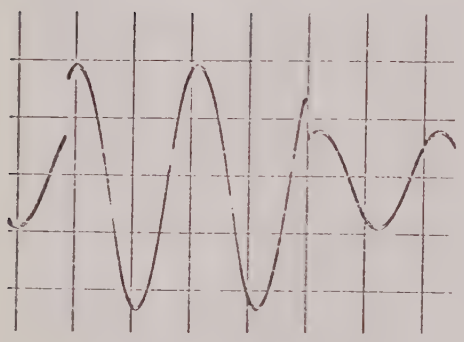
(4) Return to the TUNE (R33) control and adjust until

the junction point of the large and small cycles has a minimum of distortion (See figure 4.2).

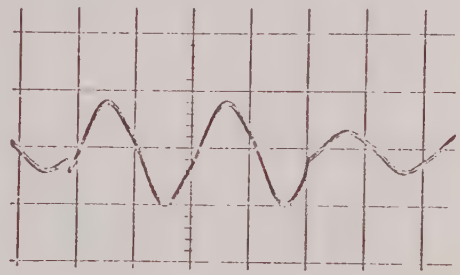
(5) Adjust the DC Code (R23) amplitude control for a nominal output of 3 V peak-to-peak.

NOTE

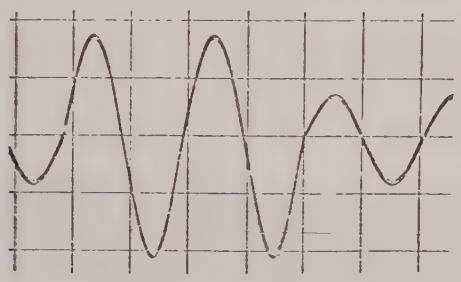
For Shaper and Modulator Dwg. #21556-7-2 or 5 item (1) should read [Adjust the TUNE (R33)---] and item (4) should read [Return to the TUNE (R33)---]



Incorrect
Adjust Tune Control CW



Incorrect
Adjust Tune Control CCW



Correct

FIGURE 4.2
Tune Control Adjustment

CHAPTER 5

FUNCTIONAL DESCRIPTION

5.1 GENERAL

Basically the Model 8120 is a precise digital clock with circuits to generate serial time codes for recording on magnetic tape or central timing application. The time codes of the standard Model is of the IRIG format. Other codes can be supplied as options.

5.2 FUNCTIONAL

For the following discussion refer to the Wiring Block Diagram.

At the right side of the drawing is shown the Time Base module A16. The card contains the 1 MHz oscillator with an amplifier shaper to shape the 1 MHz for driving i.e., decade divider circuits. This card also contains a start/stop flip-flop which is used to control the elapsed time mode of operation. On this card are also three decade dividers which divide the 1 MHz down to 1 kHz to drive the other modules in the unit.

The 1 kHz signal from this card drives the Minor Counter Module A15. Module A15 is the milliseconds card. Basically, it is a three decade divider which takes the 1 kHz input and divides it down to one pulse per second to drive the time of day accumulator. Also, when the milliseconds option is used, this module will have buffer amplifiers to isolate the decades from the external circuits.

The 1 pps signal from A15 is fed to the time of day accumulator A9 where it is divided into units of seconds, tens of seconds, units of minutes, tens of minutes, units of hours, and tens of hours. This is the module that controls the read out and feeds the information code generator module A14. The BCD time of day information also goes to the module A11 where it is buffered and supplied to J6 for external use. The dividers on this card are the type that can be parallel set from the preset switches. This allows the clock to be set to any time of day.

The parallel BCD information from this card can go to three places.

(1) to the read out drivers,

(2) to A11 which contains buffer amplifiers to drive external loads,

(3) to A14, the code generator card where the level shift time code is generated.

The output of the Code Generator (A14) goes to the modulator card (A3) to modulate the carrier with the time code information

The Modulator card has circuits to take the square wave signals of the carrier frequency and generate the sine wave carrier This card also has circuits that are used with the Days/ID option. This circuit using a switch (S15) on the rear panel selects where the Days module (A1) is up dated from, either the time of day carry or from an external source.

CHAPTER 6

CIRCUIT DESCRIPTION

TABLE 6-1

CARD LOCATION

LOCATION	CARD
A1	Days Accumulator
A2	Blank
A3	Shaper and Modulator
A4	Extender Board
A5	Blank
A6	Blank
A7	Blank
A8	Blank
A9	Time of Day Accumulator
A10	Blank
A11	Buffers
A12	Blank
A13	Blank
A14	Code Generator
A15	Buffered Accumulator/Minor Counter
A16	Time Base Preset/Reset Control

All plug-in modules are designed so that the card will only fit into position if it is correctly aligned; however, caution must be exercised to insure that a card is installed in the correct card slot. Latching handles on all cards are numbered to facilitate correct installation.

CAUTION

When mounting a card on the extender board it is possible to install the card backwards which will result in serious damage.

6.1 AC/DC POWER SUPPLY Dwg. #31357-7-1

General

The power supply produces four voltages from a switching regulator controlled DC to DC converter. The voltages are +15, -15, +5, and +210 volts dc. The input to the supply is from either 115/230 V ac or a dc source of 20 to 50 V (28 V nominal). Changeover from ac to dc operation is instantaneous.

Note: Components located on power supply board 31319-4-1 are described with the prefix A1 added. Those on term BD 31320-4-1 have A2 added.

Input Circuit

For ac operation, T1 steps down the line voltage. Diodes CR3 and CR4 provide wave rectification of the voltage and apply it to filter capacitors C1 and C2.

For dc operation, the input is connected to J2. Diode CR2 is for protection if the dc polarity if incorrect. Diode CR1 allows the dc source to supply current when insufficient voltage is available from the ac supply. Automatic battery charging is provided, via R2, when the ac power is on.

Switching Regulator (Assembly #31319-4-1)

The switching regulator accepts an input of 20 to 50 volts dc and supplies a regulated voltage of approximately 15 V to the DC to DC converter. Transistor A1-Q6, Zenner Diode A1-CR6, and potentiometer A1-R11 form an adjustable constant current source. The current generated flows through A1-R13, producing a constant voltage across the resistor. In this way, the voltage at A1-Q5 base follows the regulated voltage, with an adjustable offset. This voltage is applied to the Schmitt Trigger (A1-Q3 and A1-Q4) through emitter follower A1-Q5

The Schmitt Trigger causes A1-Q2 to conduct when the voltage drops below the set point. This causes A1-Q1 to conduct and allows Q1 to produce a pulse of voltage. The voltage pulse is applied to capacitors C3 and C4 through inductor L1. Diode CR5 is a fast recovery type used to provide a path for the voltage induced in L1 when Q1 turns off. When the voltage rises to the set point, the Schmitt Trigger turns off, terminating the voltage pulse.

Thus a series of pulses is produced which cause the voltage to oscillate about the set point. The network composed of L1, C3, and C4 smooth the pulses to produce a steady voltage. Zenner diode A1-CR5 turns off the regulator when the input voltage drops too low to maintain the output voltage.

DC TO DC CONVERTER

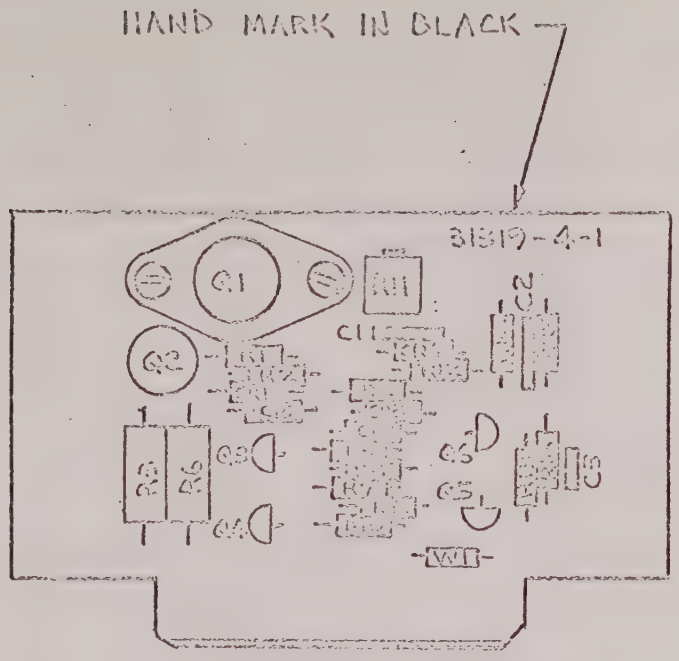
The dc voltage from the switching regulator is applied to center point of the collector winding of T2. Bias for the base winding center point is provided by A2-R4, A2-R3, and A2-CR2. A2-Q2 and A2-Q3 along with T2 form a free running oscillator which produces square wave ac on three output windings. One winding supplies +5 V through full wave rectifier CR6 and CR7; another +210 V through bridge rectifier A2-CR8-A2-CR11; and a third +15 V and -15 V through full wave rectifiers A2-CR4/A2-CR6 and A2-CR5/A2-CR7. Filter capacitors A2-C1-A2-C4 smooth the various voltages.

Adjustments

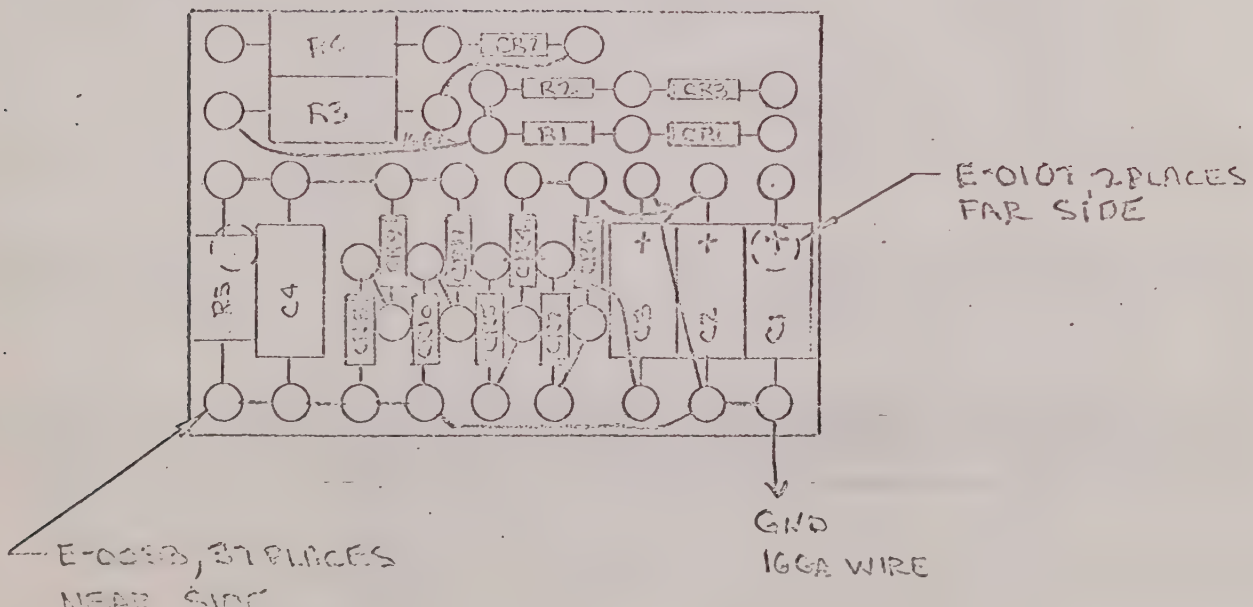
The only adjustment is A1-R11. It is set to give 5 V ±0.5 V at fuse F1 with unit operating normally.

PARTS LIST

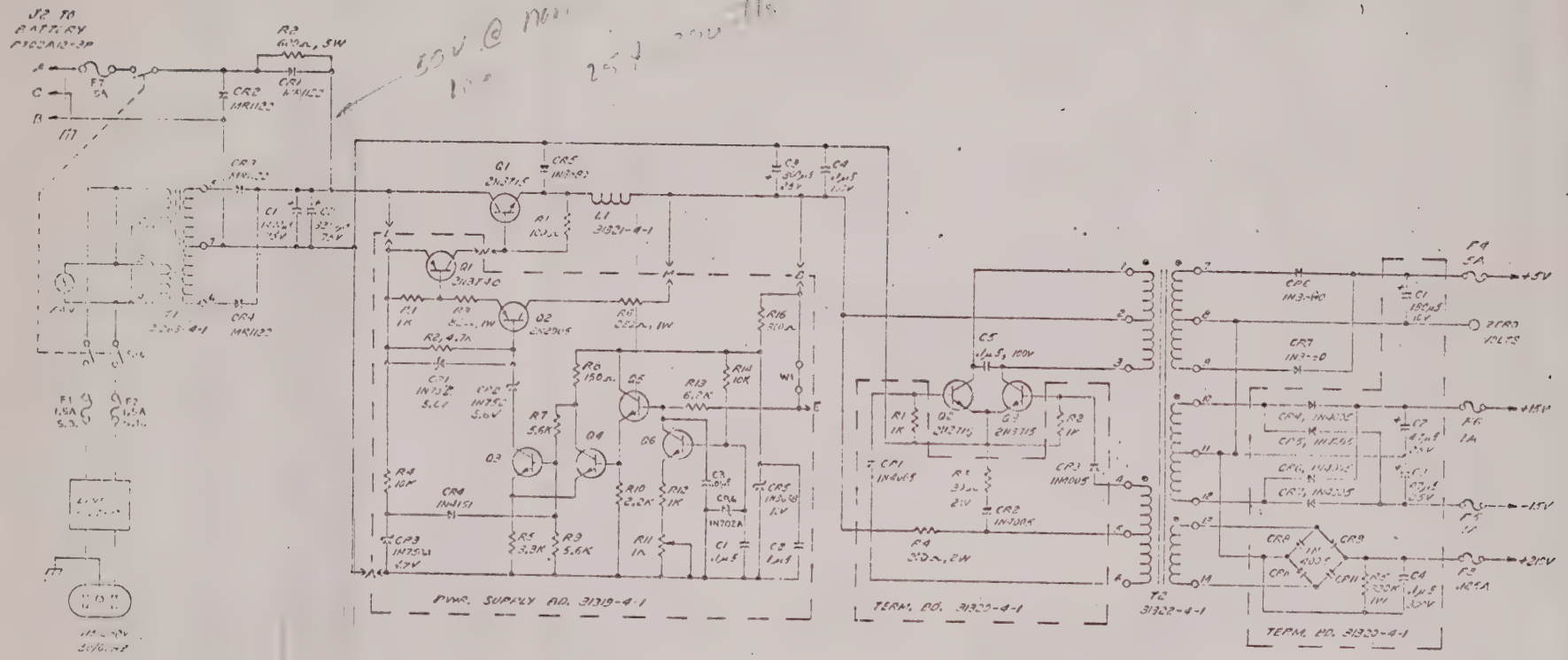
Ref.	Description	S-D Part No.
	Assembly Board	31319-4-1
	Assembly Terminal Board	31320-4-1
	Schematic Power Supply	31357-7-1
C1	Capacitor, 1400 µf, 75 V	
C2	Capacitor, 3250 µf, 75 V	
C3	Capacitor, 300 µf, 25 V	
C4,5	Capacitor, 0.1 µf, 600 V	C-0791
CR1,2,3,4	Diode, (MR 1122)	
CR5,6,7	Diode, (IN3880)	
L1	Inductor	31321-4-1
Q1,2,3	Transistor, 2N3715	Q-0223
	Socket Transistor, MK21	H-1859
R1	Resistor, 100Ω, 1/4 W, 5%	R-0966
R2	Resistor, 600Ω, SW DALE RH5	
T1	Transformer	31263-4-1
T2	Transformer	31322-4-1
	Connector, PC 12 Pin	J-0561
	Clamp Capacitor, 1-3/8 Diameter	H-0827
	Clamp Capacitor, 2 Diameter, Sangamo DCM-05	
	Clamp Capacitor 2-1/2 Diameter, Sangamo DCM-10	



ASSEMBLY
SWITCHING
REGULATOR
31319-4-1



ASSEMBLY
TERMINAL
BOARD
31320-4-1



NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS: 5%, 1/2, C.C.
2. TRANSISTORS: 2N4124.

AC/DC
POWER
SUPPLY
31357-7-1

6.2 3 DIGIT ACCUMULATOR W/BUFFERS (Dwg. #21547-7-8)

General

This card contains three decade dividers with buffered outputs. An input circuit is also provided.

Decade Dividers

Each divider performs a division by ten. The accumulator will count to 999. Provision is made to preset the decades by grounding the appropriate data input lines on each decade. The information will be loaded into the accumulator when a ground is applied to the $\overline{\text{PRESET}}$ line. Gates A8-8 and A8-3 double invert and buffer the $\overline{\text{RESET}}$ line (a ground on pin 23 causes reset to 000).

Input Inhibit

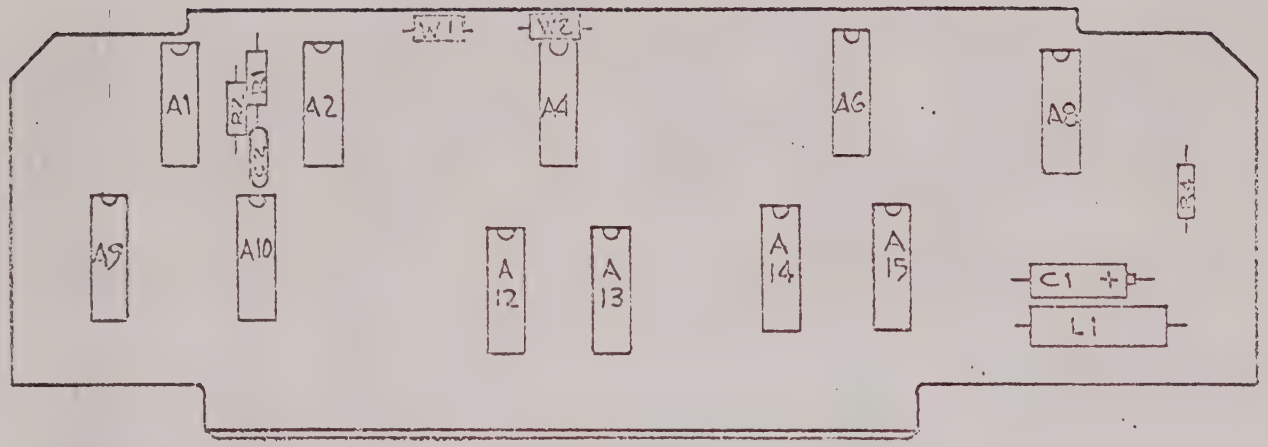
The input on pin F, is differentiated by C2 and R1/R2 and inverted by A2-6. Gates A2-3 and A2-11 double invert and buffer the inhibit input on pin H. Grounding pin H will cause the output of A2-8 to go high regardless of the output of A2-6. Thus the input is inhibited. Since the output of A2-6 is normally low (except during a negative transition on the input), the output of A2-8 will remain high when the inhibit is removed and no spurious counts will be produced.

Output Buffers

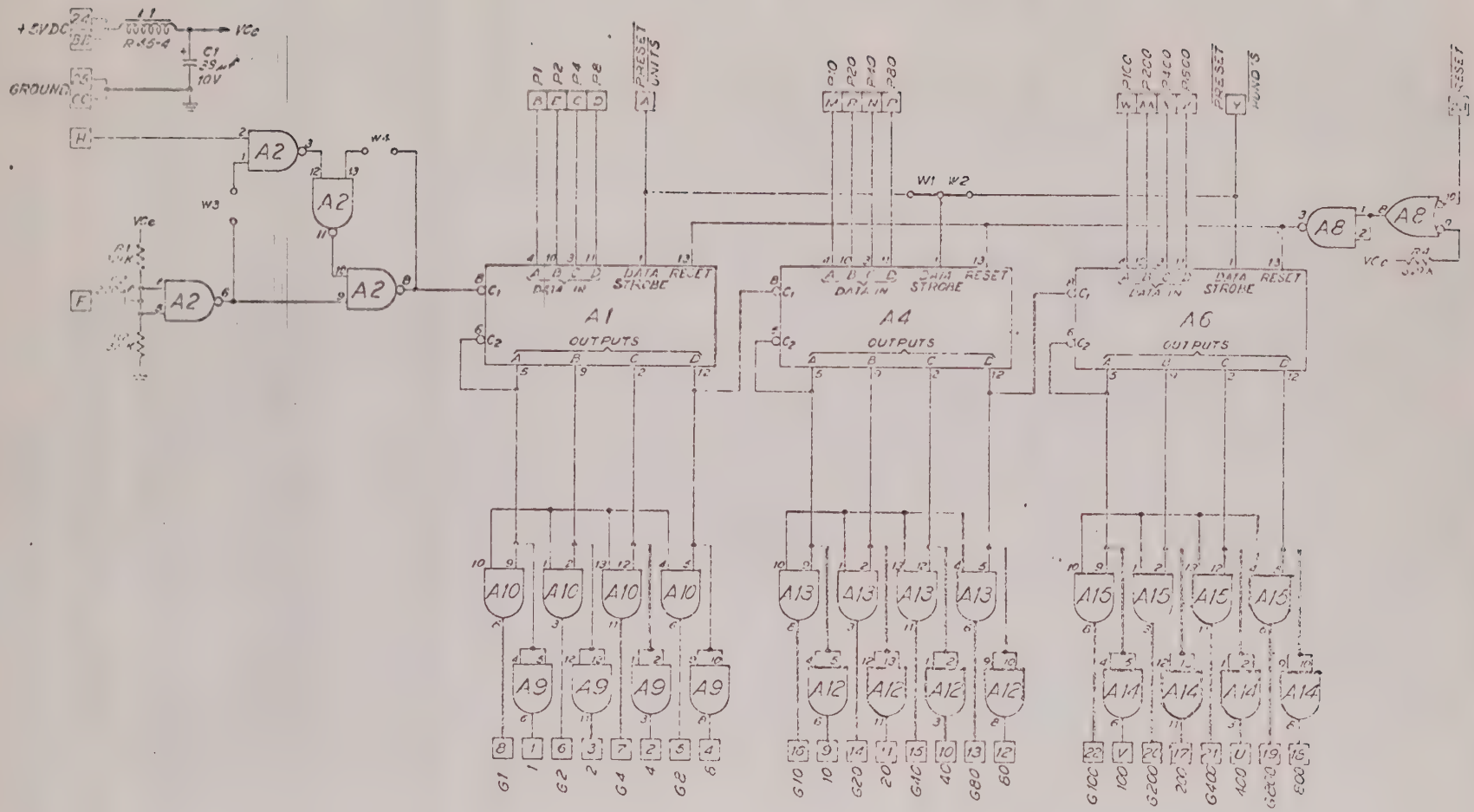
Each BCD output (coded 8-4-2-1) from the decades is connected to two output buffers. Each buffer is non inverting. The buffer outputs are 5 V logic levels from a 6 kΩ source, 15 mA sink.

PARTS LIST

Ref.	Description	S-D Part No.
	Assembly	21547-4-8
	Schematic	21547-7-8
A1,4,6	IC N8280A	25722
A2	IC MC846P	19716
A8	IC SN7400N	19705
A9,10,12,13,14,15	IC MC1806P	25733
C1	Capacitor 39 µf, 10 V TANT	C0902
C2	Capacitor 220 pf, 500 V DM	C0538
L1	Inductor R45-4	L0143
R1,2,4	Resistor 3.9 kΩ, 1/4 W, 5%	R0939
W1,2	Jumper, Molded	W0087
	Ejector	H1743



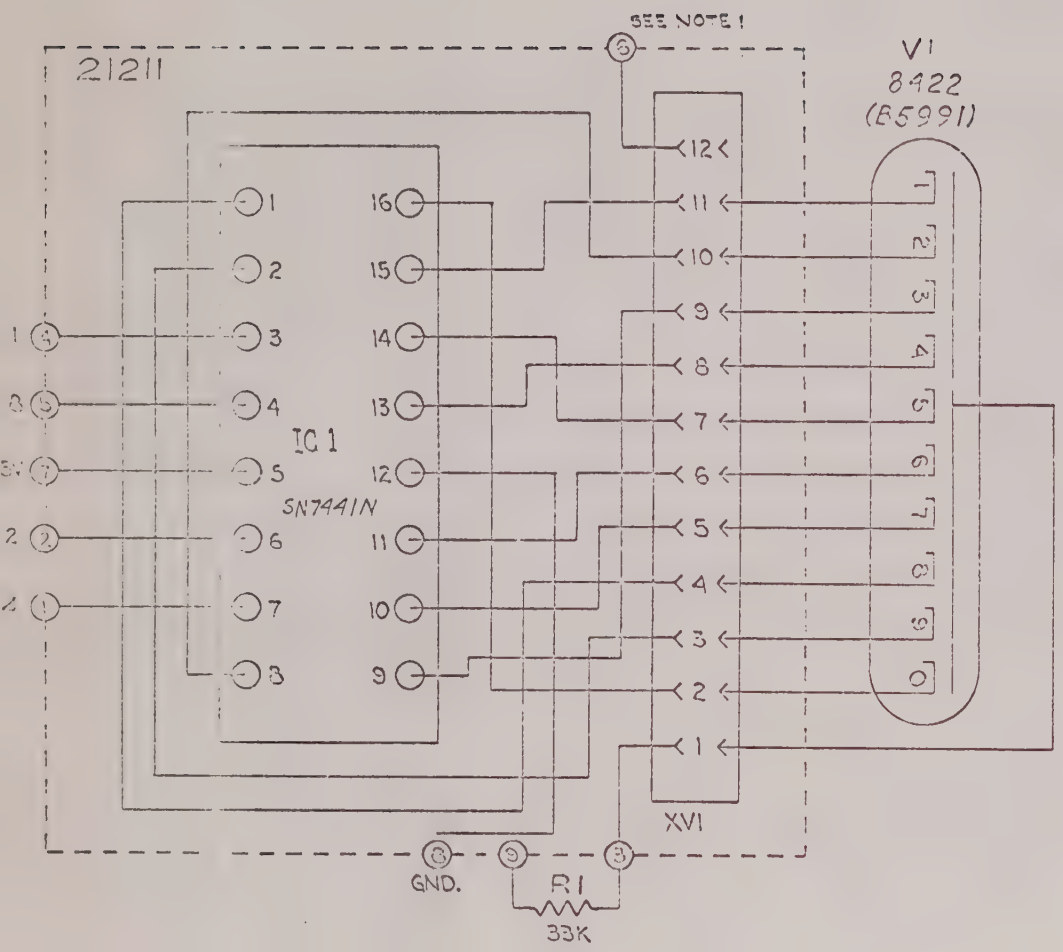
ASSEMBLY
3 DIGIT
ACCUMULATOR
W/BUFFERS
21547-4-8

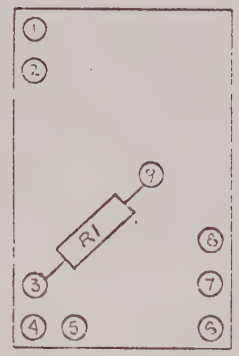


SCHEMATIC
3 DIGIT
ACCUMULATOR
W/BUFFERS
21547-7-8

6.3 SINGLE DIGIT READOUT

Ref.	Description	Part Number
	Rectangular P.C. Socket, Burroughs	X-0161
IC	TI SN744IN	19707
RI	Resistor, 33K, 5%, 1/2W, Comp Carb	R-0262





CIRCUIT SIDE VIEW

NOTE:
1. PIN 6 IS INTERNAL DECIMAL POINT WHEN V1 IS B5956

SCHEMATIC
SINGLE DIGIT
READOUT

6.4 TIME BASE PRESET/RESET CONTROL Dwg. #21555-7-6

General

The Time Base section of the card generates the 1-MHz reference signal and repeatedly divides it by 10 to provide a 100 k pps, 10 k pps, and a 1 k pps signal.

Time Base

The Time Base Generator section consists of an unheated crystal, Y1, and feedback amplifier Q1. The oscillator's output, at pin Y, may be utilized as an external 1 MHz reference or it may be jumpered to pin W for internal use. An external 1 MHz reference signal may be used instead by applying it to pin W.

The 1 MHz input is applied to the base of voltage-amplifier Q2 (which has a gain of three), isolated, and applied to the base of Q3. Clipper-circuit Q3 provides a 5 V p-p 1 MHz square wave which is gated by A4-6 into the first divide-by-ten circuit, A6. A7 and A5 also divide-by-ten (divide-by-five-then-by-two) which yields a 1 k pps symmetrical output at pins 10 and 9. 10 k pps and 100 k pps symmetrical outputs are available on pins 15 and 18 and on pin 20 respectively.

When a Logic 0 (ground) is applied to the External Stop line, flip-flop A3-9 will generate a Logic 0, which will inhibit the 1-MHz signal to the first divide-by-ten circuit. A positive transition on Pin R, the Stop Time signal, will also inhibit the clock if pin S is at ground. A ground signal on the START pin P, will clear the inhibit from A4-4. The Elapsed Time

signal, Pin 14, may also be used to stop the clock by application of a Logic 0 signal.

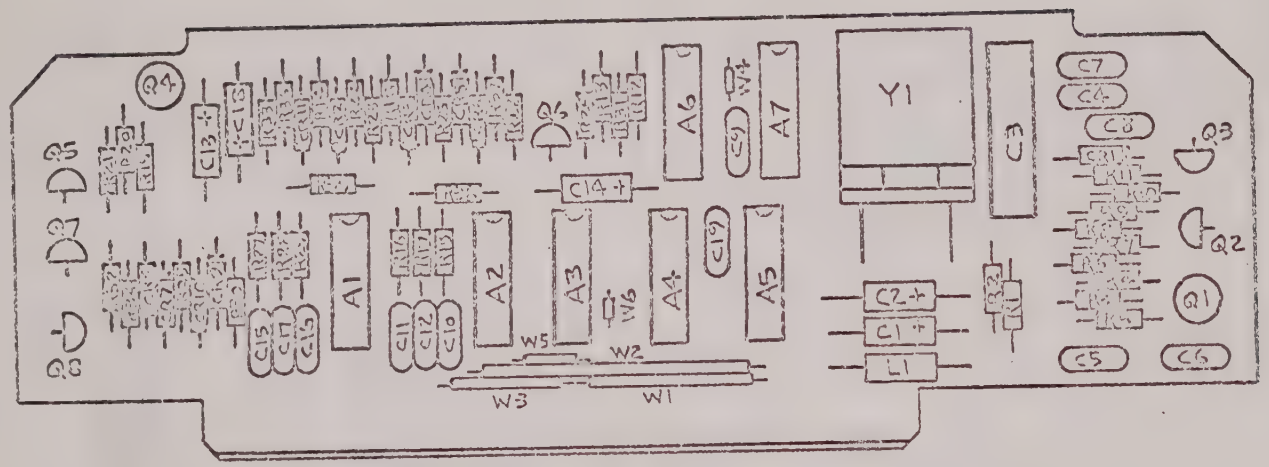
Pin 19, the Reset signal, will cause the three divide-by-ten circuits to clear to an all-reset state. Pin 19 must be grounded if not used.

Flip-flop A3-5 is used to provide the symmetrical 1 k pps.

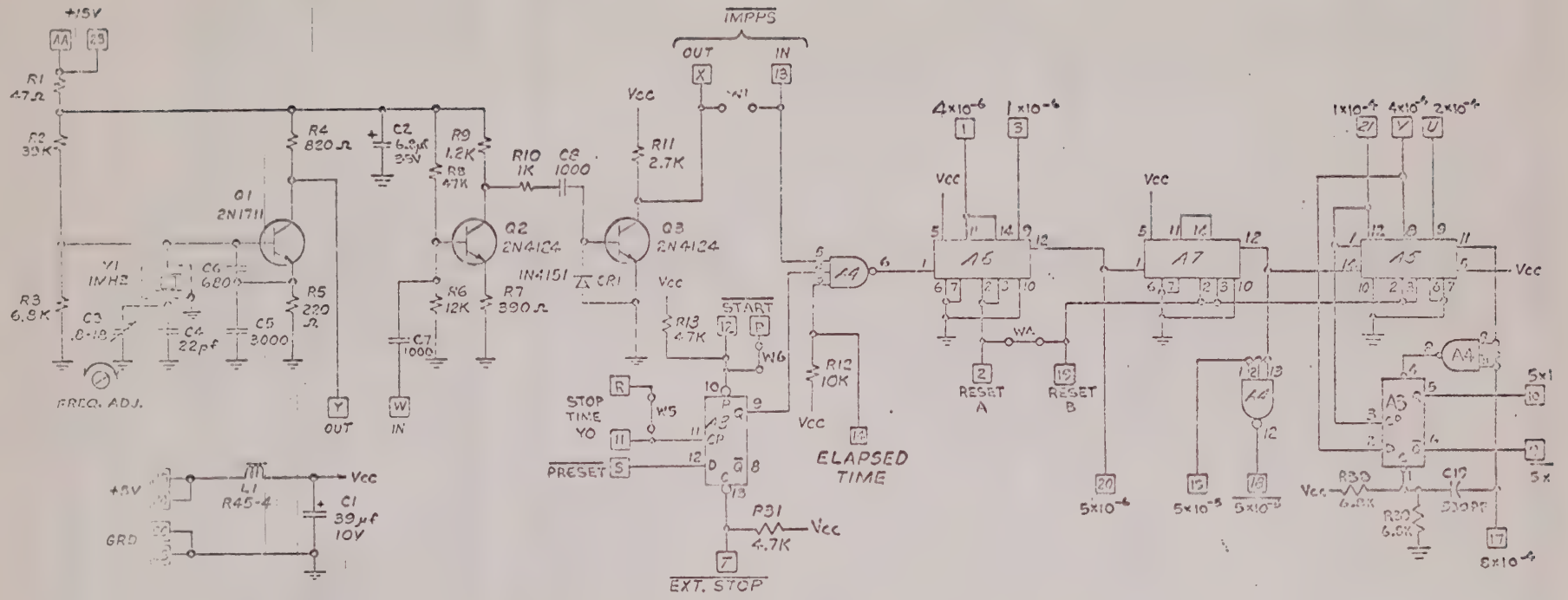
Ref.	Description	Part Number
	Assembly Schematic	21555-4-6 21555-7-6
A3	IC SN7474N	25241
A4	IC SN7410N	19706
A5-7	IC SN7490N	19711
C1	Capacitor, 39 µf, 10 V, Tant	C-0902
C2	Capacitor, 6.8 µf, 35 V, Tant	C-0899
C3	Capacitor, 0.8-18 pf, Var.	C-0555
C4	Capacitor, 22 pf, DM15	C-0378
C5	Capacitor, 3000 pf, DM19	C-0759
C7,8	Capacitor, 1000 pf, M15	C-0543
C19	Capacitor, 330 pf, DM15	C-0540
CR1	Diode, IN4151	CR-0150
L1	Inductor, R45-4	L-0143
Q1	Transistor, 2N1711	Q-0140
Q2,3	Transistor, 2N4124	Q-0235
R1	Resistor, 47Ω, 1/4W, 5%	R-0743
R2	Resistor, 39 kΩ, 1/4W, 5%	R-0748
R3,38,39	Resistor, 6.8 kΩ, 1/4W, 5%	R-0696
R4	Resistor, 820Ω, 1/4W, 5%	R-0762
R5	Resistor, 220Ω, 1/4W, 5%	R-0760
R6	Resistor, 12 kΩ, 1/4W, 5%	R-0759
R7	Resistor, 390Ω, 1/4W, 5%	R-0761
R8	Resistor, 47 kΩ, 1/4W, 5%	R-0777
R9	Resistor, 1.2 kΩ, 1/4W, 5%	R-0809

PARTS LIST (continued)

Ref.	Description	Part Number
R10	Resistor, 1 kΩ, 1/4W, 5%	R-0765
R11	Resistor, 2.7 kΩ, 1/4W, 5%	R-0937
R12	Resistor, 10 kΩ, 1/4W, 5%	R-0766
R13,31	Resistor, 4.7 kΩ, 1/4W, 5%	R-0892
W1,4-6	Jumper, 22 gage	
Y1	Crystal, 1 MHz	Y-0019
	Extractors	H-1743



ASSEMBLY
P.C. BOARD
TIME BASE
PRESET/RESET
CONTROL
21555-4



NOTE: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE IN OHMS ±5%, 1/4 W
2. CAPACITOR VALUES ARE IN pf.
3. DIODES ARE IN4151
4.
5. A3 IS SN7474N; A4 IS SN7401ON.
6. A5, A6, A7 ARE SN7490N
7. Vcc TO PIN 14, GRD TO PIN 7, ALL I.C.'S

SCHEMATIC
TIME BASE
PRESET/RESET CONTROL
21555-7-6

6.5 3 DIGIT BUFFERED ACCUMULATOR/MINOR COUNTER (Dwg. #21547-7-7)

General

The 1 k pps input signal is successively divided by 10 to provide a 1 pps signal. Buffers and an inhibit are also provided.

Decade Dividers

Decades A1, A4, and A6 successively divide the 1 k pps signal down to 1 pps. The dividers operate in a divide-by-two-then-five mode. The data inputs are not used. Gates A8-8 and A8-3 provide a buffered reset signal.

Inhibit Circuit

Gates A2 are used to allow inhibiting the 1 k pps via an external command grounding pin H will cause inhibit.

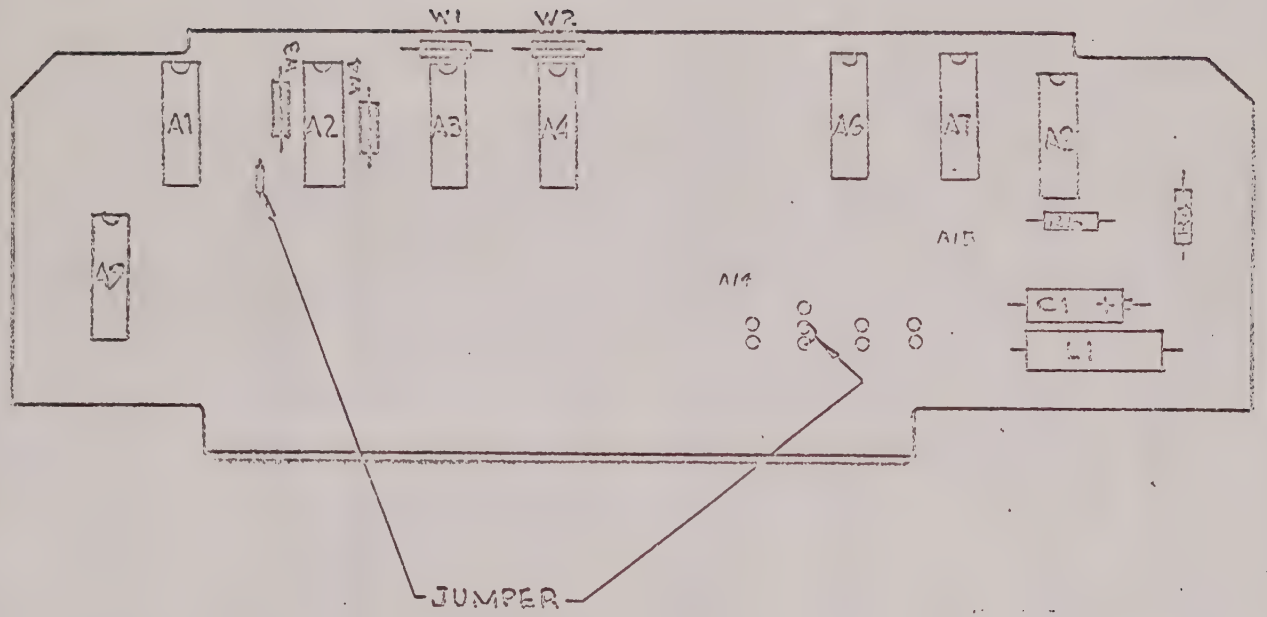
Buffers

Non inverting buffers (Gates A9) are used to provide signals (from decade A1) which are used to form the 100 Hz square wave on the shaper board.

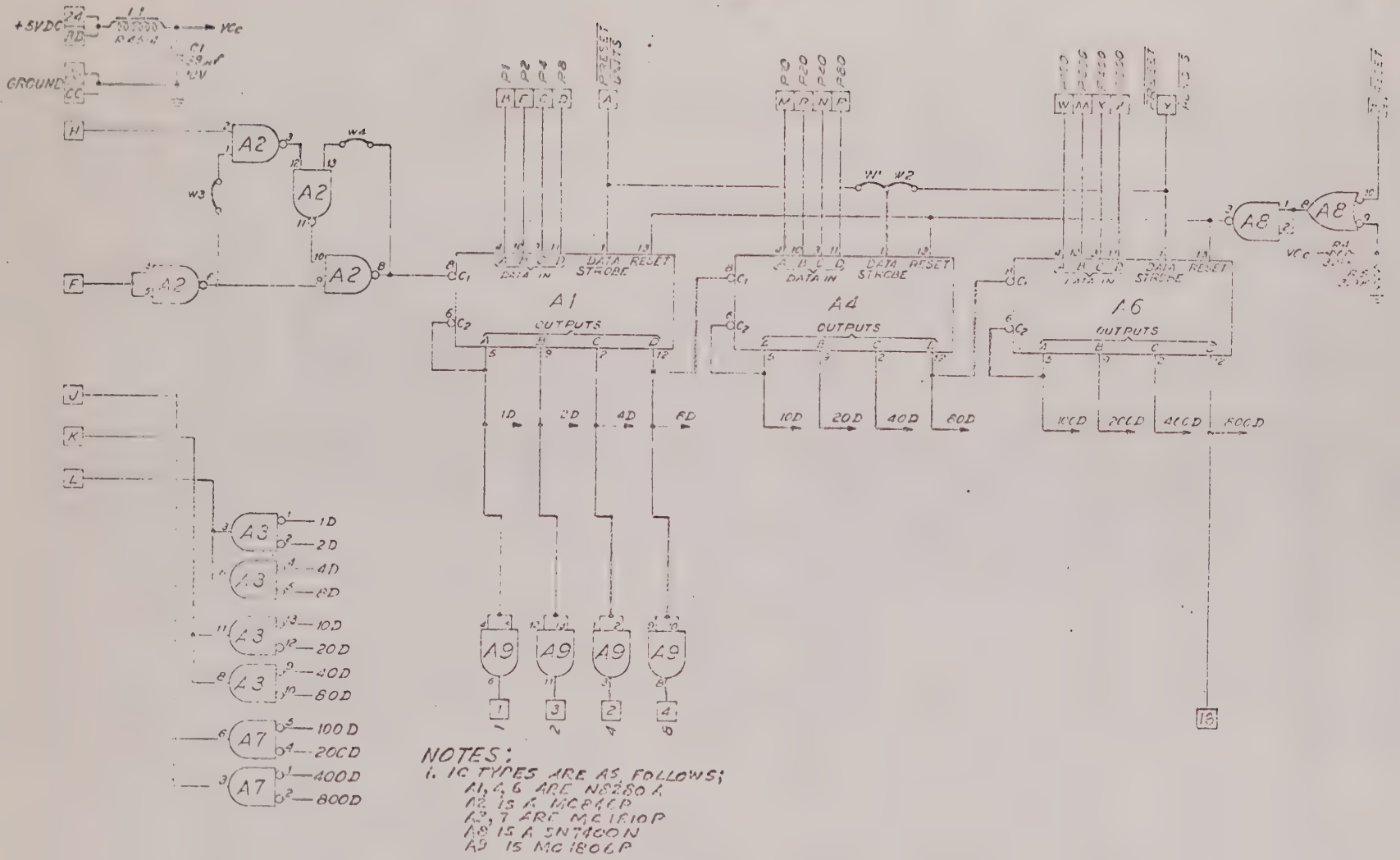
Gates A3 and A7 are used to provide three output pulse rates. The output pulse goes up on time and down at the next count within the decade.

PARTS LIST

Ref.	Description	S-D Part No.
	Assembly	21547-4-7
	Schematic	21547-7-7
A1,4,6	IC N8280A	25722
A2	IC MC846P	19716
A8	IC SN7400N	19705
A9	IC MC1806P	25733
C1	Capacitor, 39 µf, 10 V TANT	C0902
L1	Inductor, R45-4	L0143
R4,5	Resistor, 3.9k, 1/4 W, 5%	R0939
W1,2,3,4	Jumper, Molded	W0087



ASSEMBLY
3 DIGIT
BUFFERED ACCUMULATOR/
MINOR COUNTER
21547-4-7



NOTES:
1. IC TYPES ARE AS FOLLOWS;
   A1,4,6 ARE N8280A
   A2 IS A MC846P
   A3,7 ARE MC1810P
   A8 IS A SN7400N
   A9 IS MC1806P

SCHEMATIC
3 DIGIT
BUFFERED ACCUMULATOR/
MINOR COUNTER
21547-7-7

6.6 TIME-OF-DAY ACCUMULATOR Dwg. #21543-7-3

General

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, an input inhibit circuit is provided, and the hours dividers are recycled at 23:59:59.

Dividers

Dividers A2, A4, A6, and A7 divide by 10. Dividers A3 and A5 divide by 6. Each divider has its data inputs connected to the output of a preset thumbwheel switch. Grounding the appropriate preset line will load the preset time into the divider. Inverters A8 are used to buffer the reset lines.

Inhibit Circuit

The inhibit circuit is used to stop updating of the accumulator when the front panel mode switch is in the hold position. Gate A1-6 inverts the 1 pps input. Gates A1-11/A1-8 form an RS flip-flop. Gate A1-3 inverts the $\overline{\text{INHIBIT}}$ line. When the accumulator is updating, A1-11/A1-8 output follows the 1 pps input. When the $\overline{\text{INHIBIT}}$/ENABLE line, pin A, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$/ENABLE line.

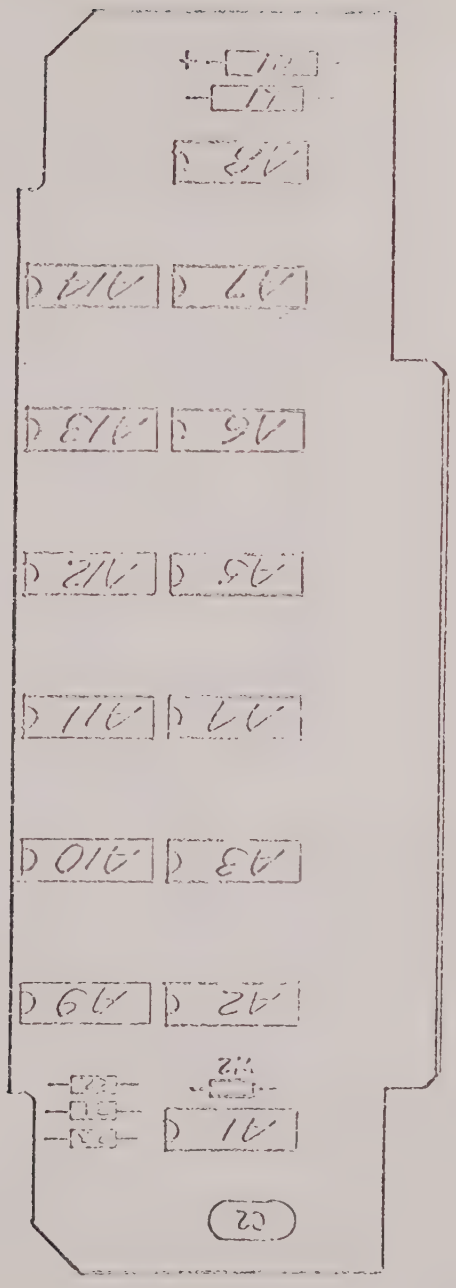
Recycle Circuit

Gates A14-6/A14-8 are connected as an RS flip-flop to control the reset lines of dividers A6 and A7 for recycle at 23:59:59.

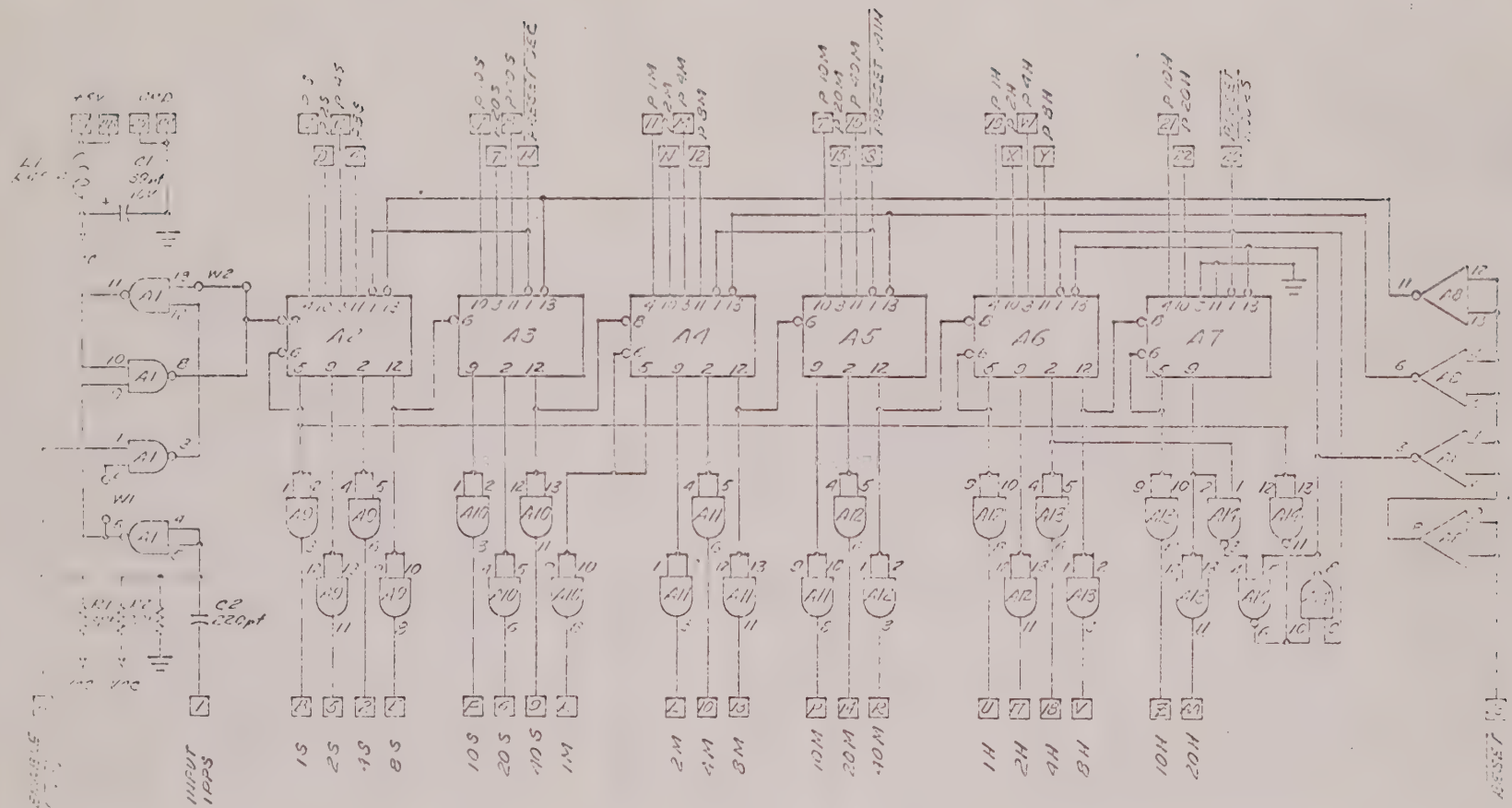
Gate A14-3 ANDS the 20 hour and the 4 hour outputs to provide a low output at 24 hours. The flip-flop (A14-6/A14-8) output will also go low, resetting A6 and A7, at this time provided the $\overline{\text{PRESET HOURS}}$ line is high. In this way, recycle is inhibited during preset. Gate A14-11 is wire AND connected to the flip-flop and maintains the reset pulse for one second. This allows all the flip-flops in the dividers time to reset. Reset may also be initiated from the $\overline{\text{RESET}}$ line via A8-3.

PARTS LIST

Ref.	Description	S-D Part No.
A1, 8, 14	IC, MC846P	19716
A2, 4, 6, 7	IC, N8280A	25722
A3, 5	IC, C2125-A	25723
A9-13	IC, MC1806P	25733
C1	Capacitor, 39 µf, 10 V	C0902
C2	Molded Jumper (See W1-3)	W0087
R3	Resistor, CC, 3.9 k, 1/4W, 5%	R0939
L1	Inductor, R45-4	L0143
W1-3	Molded Jumper	W0087
	Schematic	21543-7-3



ASSEMBLY,
ACCUMULATOR
P.C. BOARD
21543-4-3



NOTES:

PIN 7 IS CONNECTED TO GRD ON ALL I.C.'S.
PIN 14 " " " VCC " " " ".
A2, A4, A6, A7 ARE N82S0A
A3, A5 ARE Q2125-A
A1, A8, A14 ARE MC1846P
A10, A11, A12, A13, A9 ARE MC1806P

SCHEMATIC,
TIME OF DAY
ACCUMULATOR
21543-7-3

6.7 SHAPER AND MODULATOR (Dwg. #21556-7-6)

General

This card performs three primary functions:

(1) Production of modulated code on a 100 Hz carrier.

(2) Control of DC code output level.

(3) Control of Days/Run Number

In addition, buffers and inverters for two pulse rates are located on the card.

100 Hz Shaper

The 100 pps square wave from A2-11 is integrated by R29 and C14 and applied to the base of the constant current amplifier Q12. Q11 is an amplifier with C15 providing capacitive feedback. With capacitive feedback, the output (at R33) of this amplifier appears as an inductive reactance. The addition of C16 gives the circuit the electrical properties of a tuned tank circuit, with R33 used for frequency adjustment. R34 is factory selected and adds enough resistive component to the circuit to allow for a full range adjustment of R33. The signal at the gate of Q13 is a sine wave which is buffered and fed to the modulator, Q1.

Signal Outputs

R16, the MODULATION RATIO adjustment, sets the percentage of modulation before the signal is applied to pin 2 of amplifier 11.

R20, the MODULATED CODE AMPLITUDE adjustment, determines the gain of amplifier A4 and the signal level at the MODULATED CODE OUTPUT, pin X.

Q4 inverts the DC code; Q2, Q3 and the setting of R23 (the DC CODE AMPLITUDE adjustment, determine the size of the DC CODE OUTPUT) (Max signal swing +0.4 V to +10 V). CR3, CR4 and R24 provide the output with short-circuit protection, while CR3, CR5 and R25 establish the quiescent current in Q3 and Q4.

Days/Run Number Control Circuit

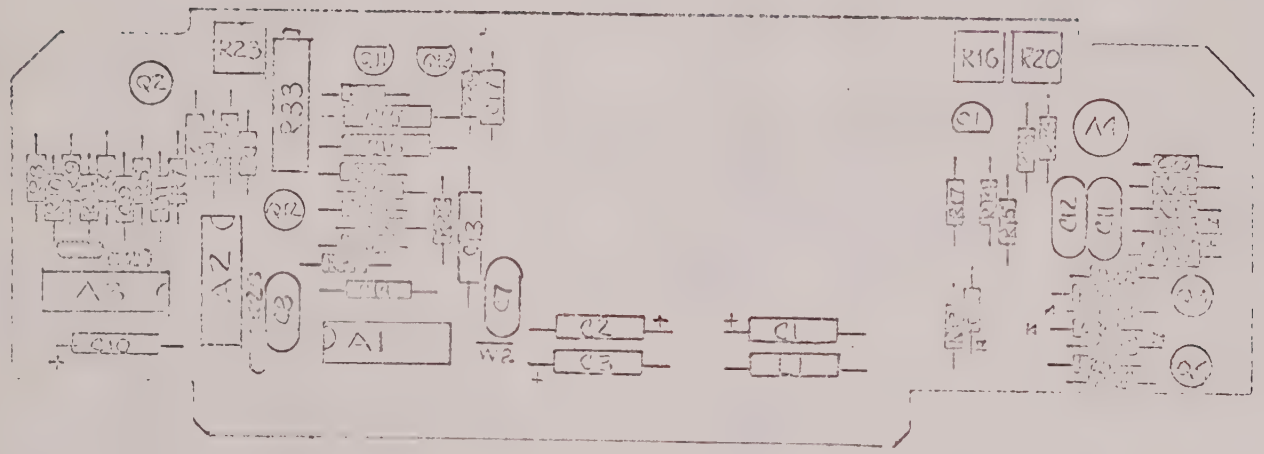
Gates A3 control the selection of the signal which is used to update the days accumulators. The carry out of the hours accumulators is inverted and applied to A3-9. If the other input (the "ID NUM" line) is high (i.e. left open), then the hours accumulator carry will update the days accumulator. Similarly, a high on the $\overline{\text{DAYS}}$ line permits a signal on pin B ($\overline{\text{ID NUM ADV}}$) to update the days accumulator. The ID advance is modified by a one shot to insure only one pulse is produced.

PARTS LIST

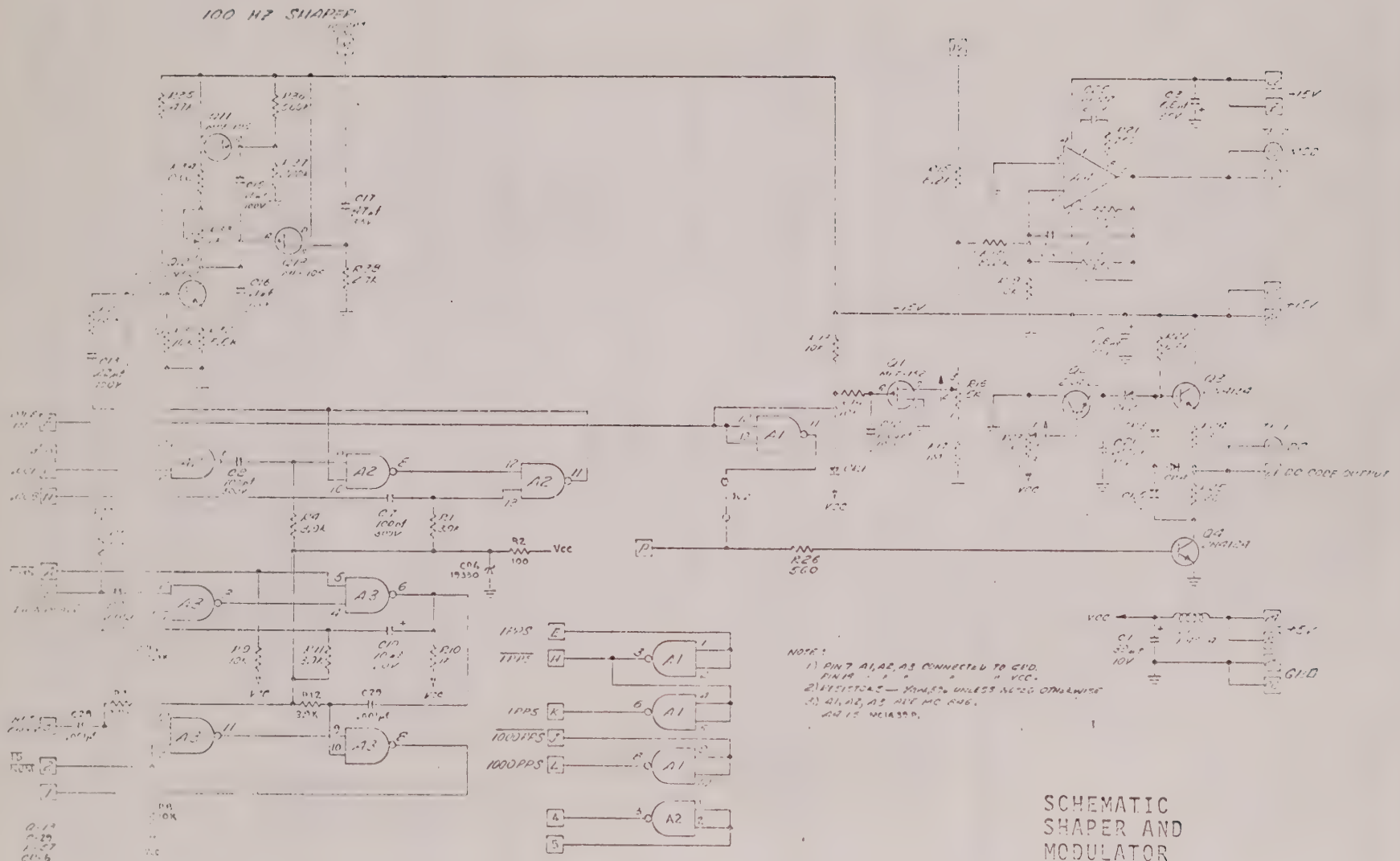
Ref.	Description	S-D Part No.
	Assembly	21550-1-6
	Schematic	21550-7-6
A1,2,3	IC MC846P	19716
A4	IC MC1439G	25729
C1	Capacitor, 39 µf, 10 V	C0902
C2,3	Capacitor, 6.8 µf, 35 V	C0899
C7,8	Capacitor, 100 pf, 500 V	C0536
C9	Capacitor, 0.001 µf, 200 V	C0717
C10	Capacitor, 10 µf, 20 V	C0353
C11	Capacitor	
C12	Capacitor, 1000 pf, 100V	C0543
C13	Capacitor, 0.22 µf, 100 V	C0746
C14	Capacitor, 0.033 µf, 100 V	C0735
C15,16	Capacitor, 0.1 µf, 100 V	C0734
C17, 26	Capacitor, 0.47 µf, 35 V	C0733
C25	Capacitor, 0.0022 µf, 200 V	C0913
C27,28	Capacitor, 0.001 µf, DISC	C0235
CR1,2,3,4,5	Diode, 1N4151	CR0150
CR6	Diode, 19330	19330
L1	Inductor R45-4	L0143
Q1	Transistor, MPF-152	Q0263
Q2	Transistor, 2N4126	Q0236
Q3,4	Transistor, 2N4124	Q0235
Q11,13	Transistor, MPF-105	Q0264
Q12	Transistor, 2N3565	Q0237
R1,4,6,7,11,12	Resistor, 3.9 kΩ, 1/4 W, 5% CC	R0939
R2	Resistor, 100 Ω, 1/4 W, 5% CC	R0966
R5,8,9,13,14,19,28,31	Resistor, 10 kΩ, 1/4 W, 5% CC	R0766
R10	Resistor, 1 kΩ, 1/4 W, 5% CC	R0765
R15,18	Resistor, 8.2 kΩ, 1/4 W, 5% CC	R0883
R16	Resistor, 5 kΩ, 62 PA VAR	R2413
R17	Resistor, 1 MΩ, 1/4 W, 5% CC	[illegible]
R27	Resistor, 100 kΩ, 62 PA VAR	R2403

PARTS LIST (continued)

Ref.	Description	S-D Part No.
R21	Resistor, 750 Ω, 1/4 W, 5% CC	R1425
R22	Resistor, 6.8 kΩ, 1/4 W, 5% CC	R0696
R23	Resistor, 10 kΩ, 62 PA VAR	R2412
R24	Resistor, 33 Ω, 1/4 W, 5% CC	R1550
R25	Resistor, 120 Ω, 1/4 W, 5% CC	R1461
R26	Resistor, 560 Ω, 1/4 W, 5% CC	R0819
R29	Resistor, 68 kΩ, 1/4 W, 5% CC	R0891
R30	Resistor, 56 kΩ, 1/4 W, 5% CC	R1235
R32	Resistor, 5.6 kΩ, 1/4 W, 5% CC	R0821
R33	Resistor, 1 kΩ, 79 P BECK	
R34	Resistor	
R35	Resistor, 47 kΩ, 1/4 W, 5% CC	R0777
R36	Resistor, 560 kΩ, 1/4 W, 5% CC	R1321
R37	Resistor, 220 kΩ, 1/4 W, 5% CC	R0967
R38	Resistor, 2.7 kΩ, 1/4 W, 5% CC	R0937
W2	#24 Insulated Wire	
	Extractor	H1743



ASSEMBLY
SHAPER AND
MODULATOR
21556-4-6



SCHEMATIC
SHAPER AND
MODULATOR
21556-7-1

6.8 SWITCHABLE IRIG DC CODE GENERATOR (Dwg. #21554-7-1)

GENERAL

This card permits generation of any one of IRIG A, B, C, or E codes. Code selection is remotely controlled. A dc level shift output is produced.

DIVIDER CIRCUITS

Refer to timing diagrams, Figures 6.1 & 6.2 for this and all following sections. Divider A8 is a divide by two then by five counter which divides down the "Z RATE" and provides decoded outputs for the code generating gates. Divider A15 is a divide by five then by two counter which takes the output of A8, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide by two then by six counter. Its principal function is to control the secondary scan gate A4. The division by twelve is used only for IRIG C, the divider being reset at the count of ten for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on sheet two is simply eliminated when the divider resets at ten. Reset at ten is established by gate A18-8. A one shot, A18-12 and A18-6 performs code frame reset. An external reset signal may be used for code frame reset when W1 is installed, or this card will supply a reset pulse to synchronize the associated accumulator when W2 is installed.

SCAN GATES

Creation of serial ones is accomplished by a two stage switching

network and a series of gates. Switches A10-A14 are basically single pole (pin 8 is the output) 8 position switches. The switching is controlled by BCD information on pins 1, 2, and 13. Since all five switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus the need for switch A4. This switch, controlled from the BCD outputs of divider A17 selects the proper time interval for serializing each switch output. The series of gates connected to A14 and A13 outputs further control those switches which have outputs that should not be present in certain codes. Tenths of seconds are added only in IRIG A, unit seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A5-8, A5-11, and A3-8 are used to inhibit the presence of serial ONES at certain times when no serial ONES should be present. This prevents the spurious "ONES" coming from the switches from appearing in the output code.

CODE GENERATING GATES

These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A 2 length is a ZERO, a 5 is a ONE, and an 8 is an INDEX MARKER. The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval.

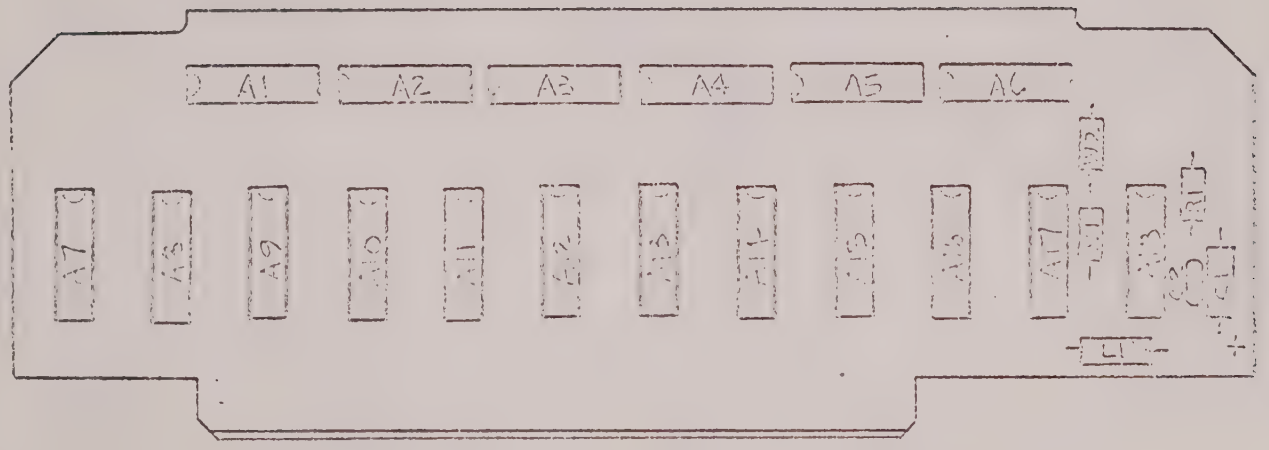
Gate A9-11 supplies a pulse of "Z" width at the start of each bit interval. If a MARKER or a ONE is not present then the output code will be high for only the "Z" width. Gate A1-6 supplies the "5" width pulse. This is AND gated with the $\overline{\text{SERIAL ONES}}$ from A13-8 by gate A1-8. The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the outputs code.

SPUR COUNTER

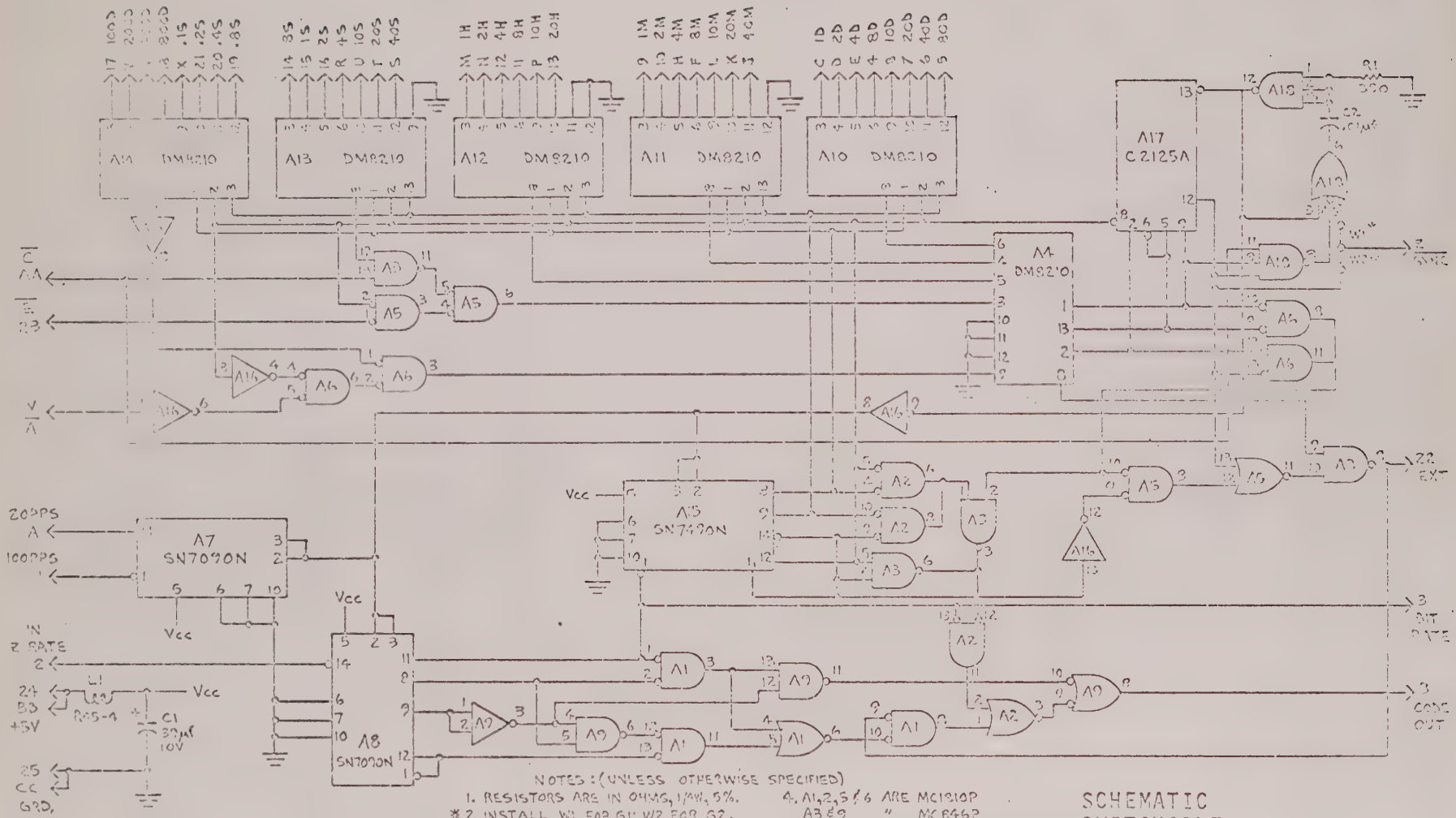
Divider A7 is included on this card to provide an additional divide by five circuit. Its primary use is in generating the IRIG C code Z rate from the 100 pps rate available elsewhere in the unit. It is synchronized with the common frame reset line.

PARTS LIST

Ref.	Description	S-D Part No.
	Assembly	21554-4-1
	Schematic	21554-7-1
A1,2,5,6	IC MC1810P	25735
A3,9	IC MC846P	19716
A7,8	IC SN7090N	25732
A4,10,11,12,13,14	IC DM8210	25746
A15	IC SN7490N	19711
A16	IC MC836P	25704
A17	IC-C2125A	25723
A18	IC SN7410N	19706
C1	Capacitor, 39 µf, 10 V TANT	C0902
C2	Capacitor, 0.01 µf DISC.	C0556
L1	Inductor, R45-4	L0143
R1	Resistor, 390 Ω, 1/4 W, 5%	R0880
W1	Jumper, Molded	W0087
	Extractor	H1743



ASSEMBLY
SWITCHABLE
IRIG DC CODE
GENERATOR
21554-4-1



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
* 2. INSTALL W1 FOR G1, W2 FOR G2.
3. PIN 7 OF ALL IC'S. IS CONN. TO GRD.
" 14 " " " " " " Vcc
4. A1,2,3,5 & 6 ARE MC1810P
A8 & 9 " MC846P
A16 IS MC836P
A18 " SN7416N

SCHEMATIC
SWITCHABLE
IRIG DC CODE
GENERATOR
21554-7-1

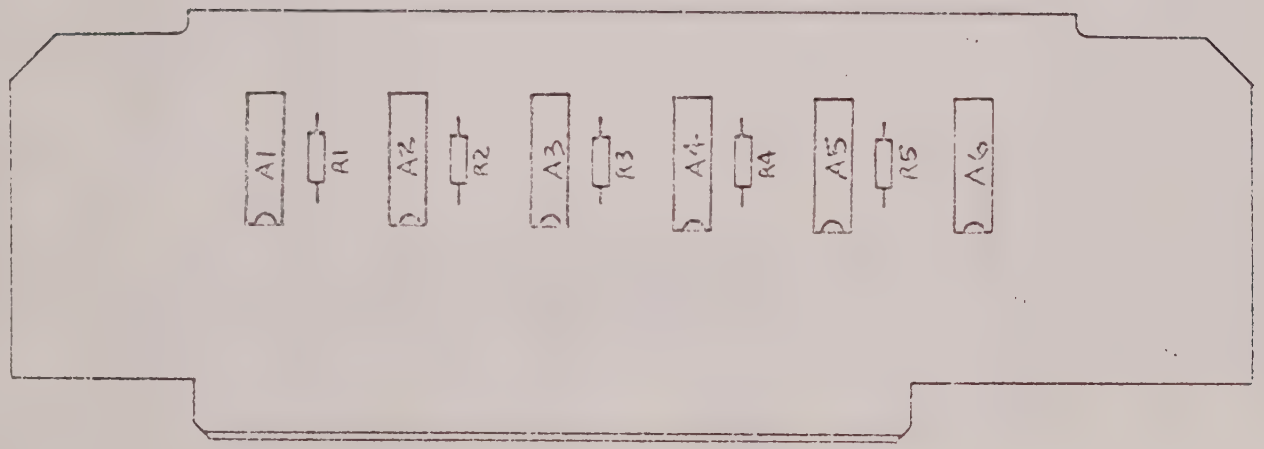
6.9 20 BIT BUFFER (Dwg. #21535-7-3)

General

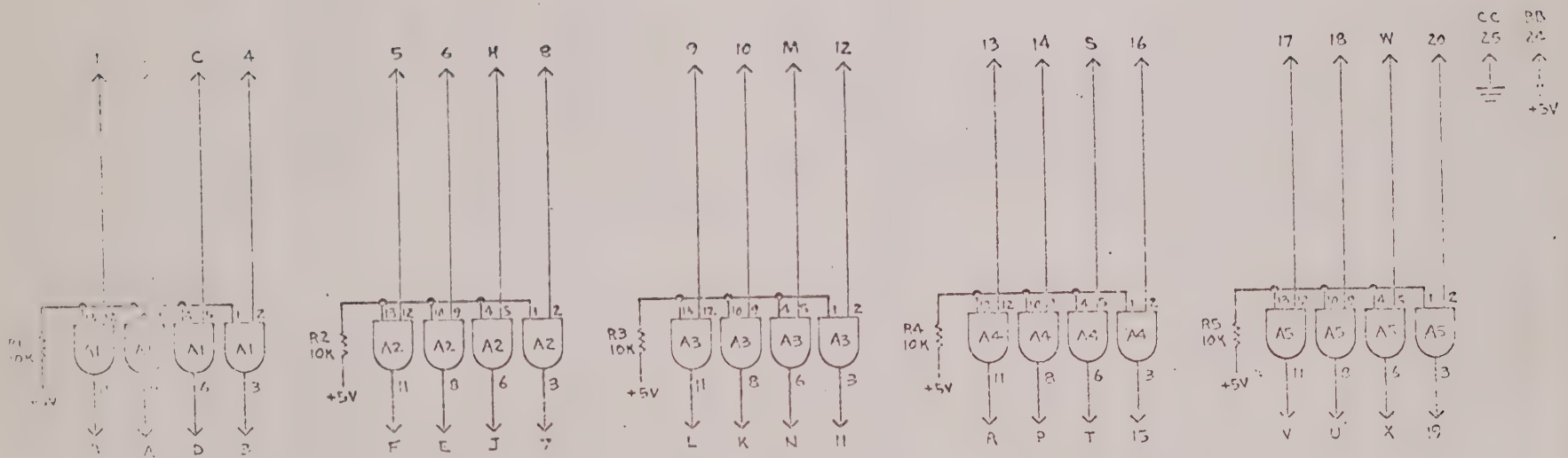
This card contains twenty Integrated Circuit gates, connected as non-inverting buffers. It is used to buffer the seconds through hours outputs of the time of day accumulators. A binary "1" output is 5 V (±0.5 V) 6 kΩ source. A binary "0" output is 0 V (±0.5 V) 15 mA sink.

PARTS LIST

Ref.	Description	S-D Part No.
	Assembly (non-inverting)	21535-4-3
	Schematic	21535-7-3
A1,2,3,4,5	IC MC1806P	25733
R1,2,3,4,5	Resistor, 10 kΩ, 1/4 W, 5%, CC	R0766
	Extractor/Roll Pin	H1743



ASSEMBLY
20 BIT BUFFER
NON-INVERTING
21535-4-3



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V &
   " 7 " " " " " " GRD.

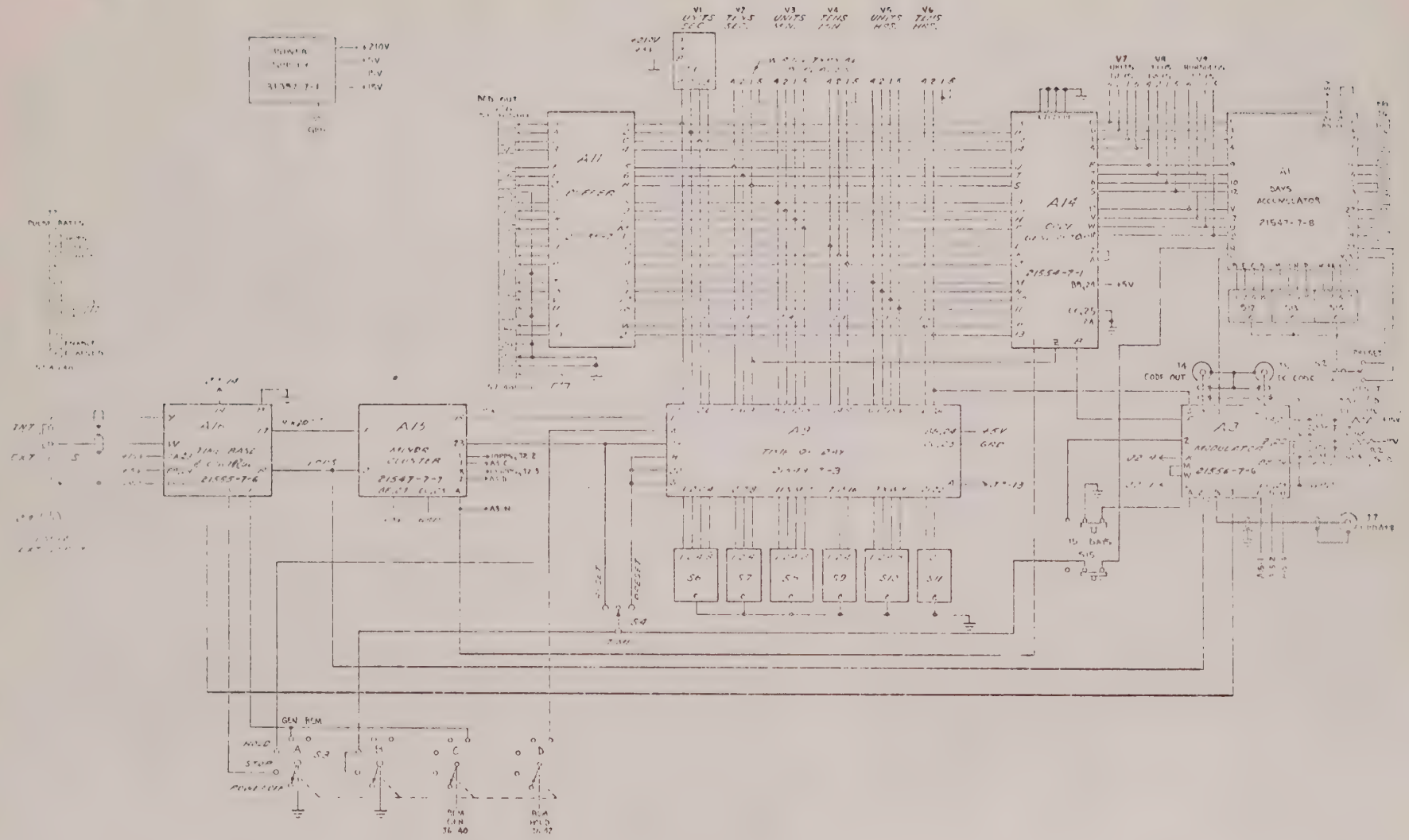
A1 THRU A5 ARE MC1800R

SCHEMATIC

20 BIT BUFFER

NON-INVERTING

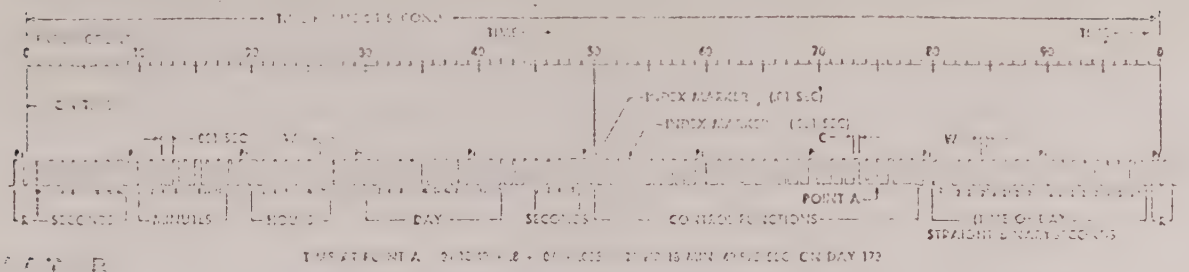
21535-7-3



WIRING
BLOCK
DIAGRAM
MODEL 8120-232
WITH IRIG C 100 Hz
31356-7-1

FORMAT B

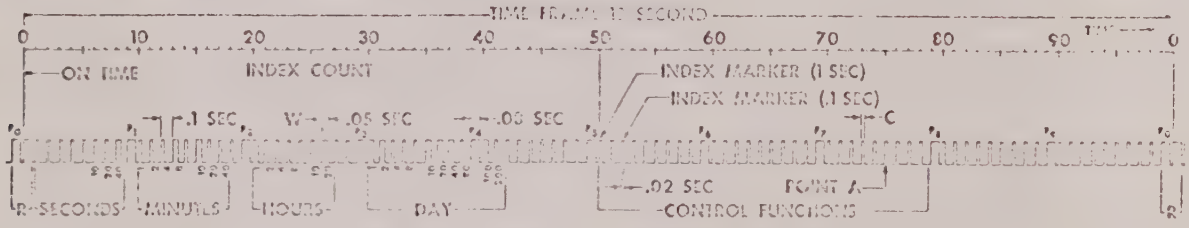
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:10:42 + .7 + .03 = 21 HRS. 10 MIN. 42.73 SEC. ON DAY 173

FORMAT E

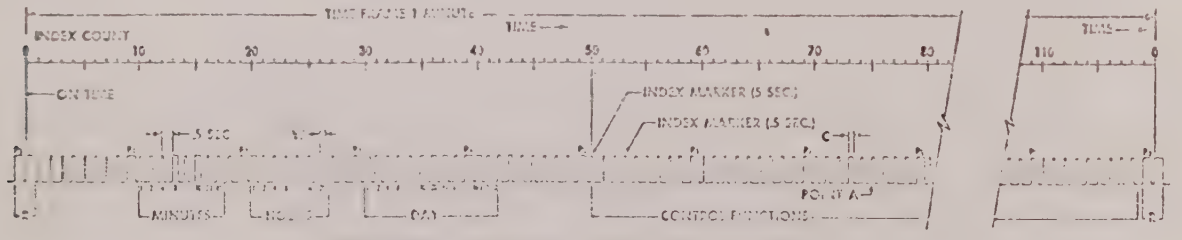
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21:10:42 + .7 + .05 + 21 HRS. 10 MIN. 42.75 SEC. ON DAY 173

FORMAT C

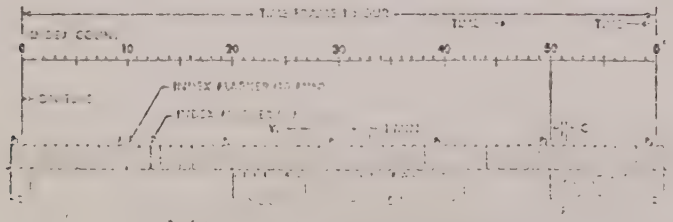
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE

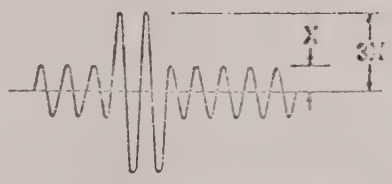


TIME AT POINT A = 21:10: + 37.5 SEC. = 21 HRS. 10 MIN. 37.5 SEC. ON DAY 173

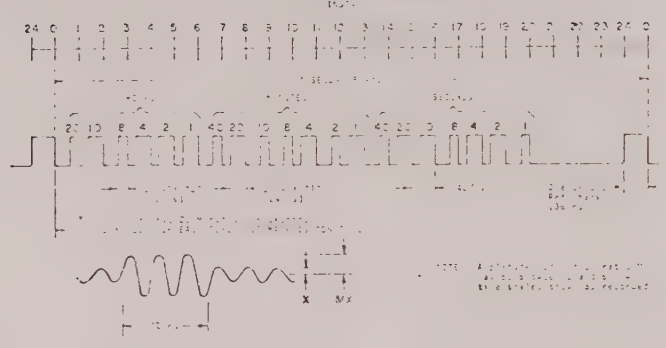
FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE

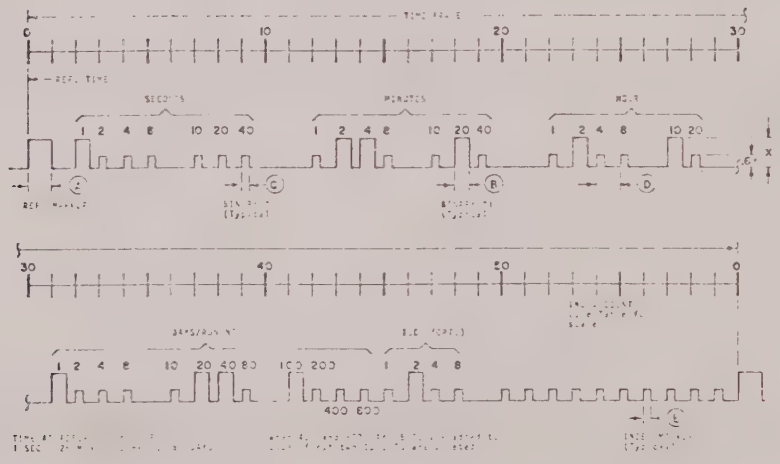


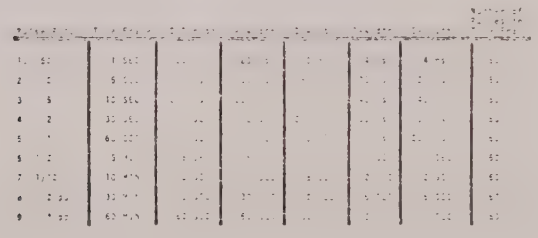


XR 3 TIME CODE FORMAT



SLOW CODE -- TYPE "B"





OPTIONAL CODES

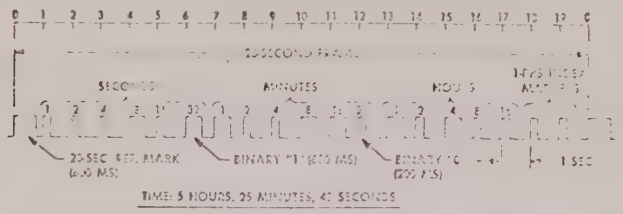
and

CODE FORMATS

AMR TIME CODE FORMATS

ATLANTIC MISSILE RANGE NO. B1

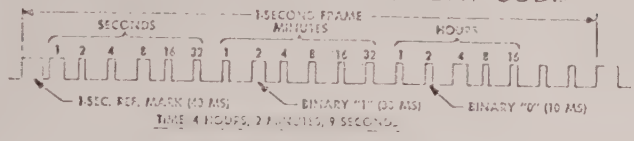
17-BIT, 1-PPS, BINARY TIME-OF-DAY CODE



TIME: 5 HOURS, 25 MINUTES, 42 SECONDS

ATLANTIC MISSILE RANGE NO. C1

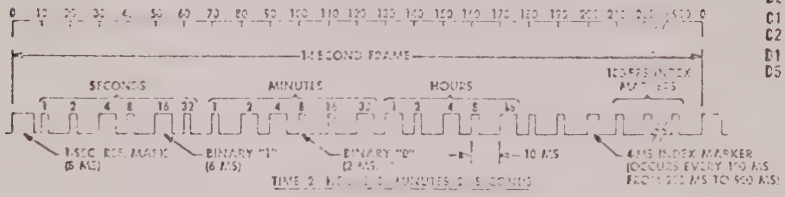
17-BIT, 20-PPS, BINARY TIME-OF-DAY CODE



TIME: 4 HOURS, 2 MINUTES, 9 SECONDS

ATLANTIC MISSILE RANGE NO. D1

17-BIT, 100-PPS, BINARY TIME-OF-DAY CODE

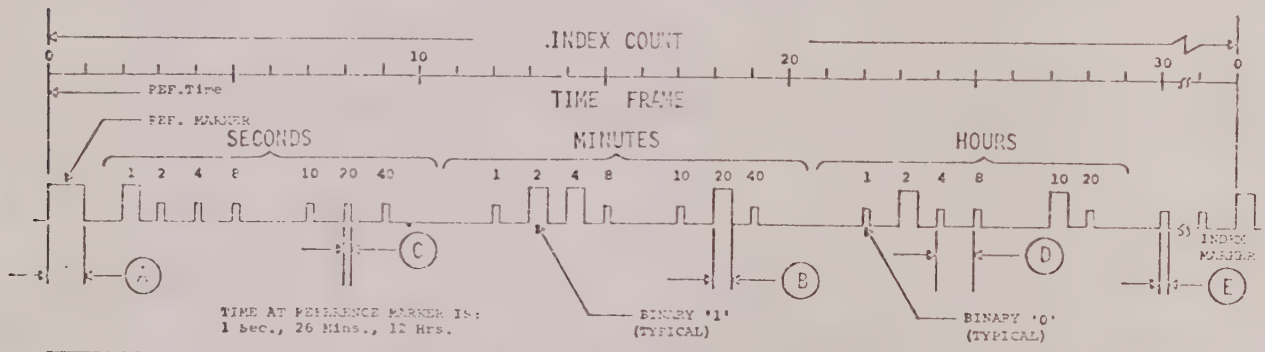


TIME: 2 HOURS, 2 MINUTES, 9 SECONDS

AMR SIGNAL DESIGNATIONS

AMR NO.	17-BIT, 24-HOUR BINARY CODE
B1	1 PPS (pulse width)
B2	1 PPS (modulated)
C1	20 PPS (pulse width)
C2	20 PPS (modulated)
D1	100 PPS (pulse width)
D2	100 PPS (modulated)

SLOW CODE - TYPE 'A'



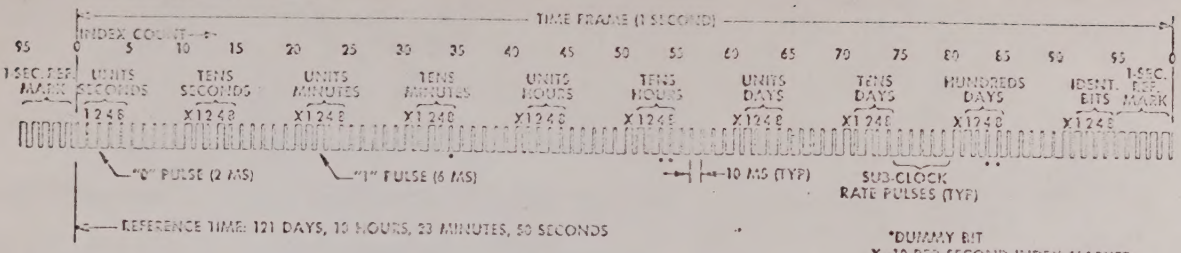
	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec.	1 Sec.	500 ms	200 ms	200 ms	30
5	1/2 pps	60 Secs.	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1/10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs	2 Secs	2 Secs	30
7	1/20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs	4 Secs	4 Secs	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs	12 Secs	12 Secs	30
9	1/2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min	24 Secs	24 Secs	30

REFERENCE MARKER = 100% OF PERIOD
BINARY "1" = 50% OF PERIOD
BINARY "0" = 20% OF PERIOD
BINARY "1" AMPLITUDE = + 10V DC
BINARY "0" AMPLITUDE = + 6V DC

OPTIONAL CODES
and
CODE FORMATS

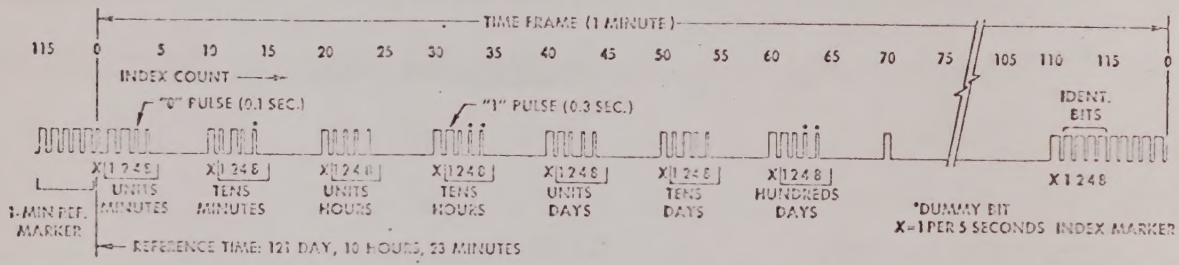
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES



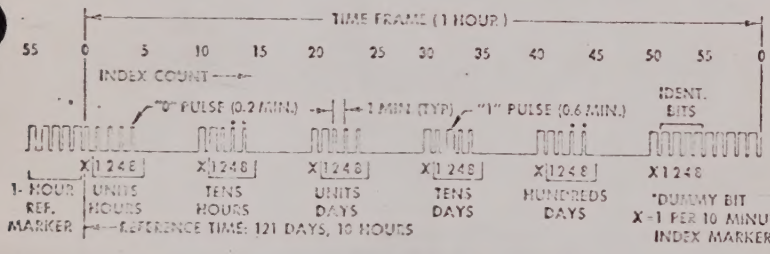
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED

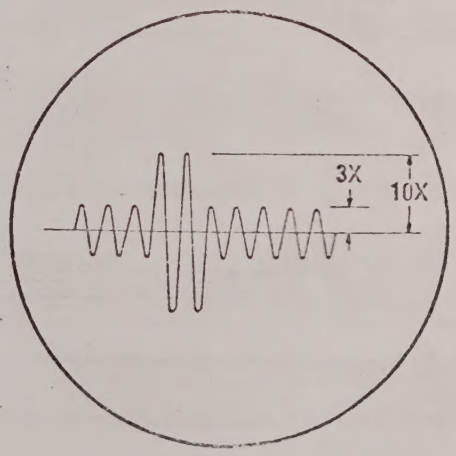


20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED



Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



TYPICAL MODULATED SIGNAL

OPTIONAL CODES

and

CODE FORMATS

Units/sec
1
2
4
8
Tens/sec
1
2
4

MP MASTER
MA33989